

MS-7509

uATX(244mm X 200mm)

CPU:

AMD AM2+ Socket940

System Chipset:

North Bridge --- / MCP78

South Bridge --- NA

OnBoard Chipset:

Clock Gen:NA

AC'97 Codec:ALC888

LAN Chip: REL8211BL/8201CL

SIO:Fintek 882(with smart fan control-3/4 pin co-lay)

Flash ROM:8MB SPI (SIO)

Main Memory:

DDRII* 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 1

PCI Slot * 2

PWM:

Controller:ISL6566

ACPI:

UPI solution

Other:

FDD *1

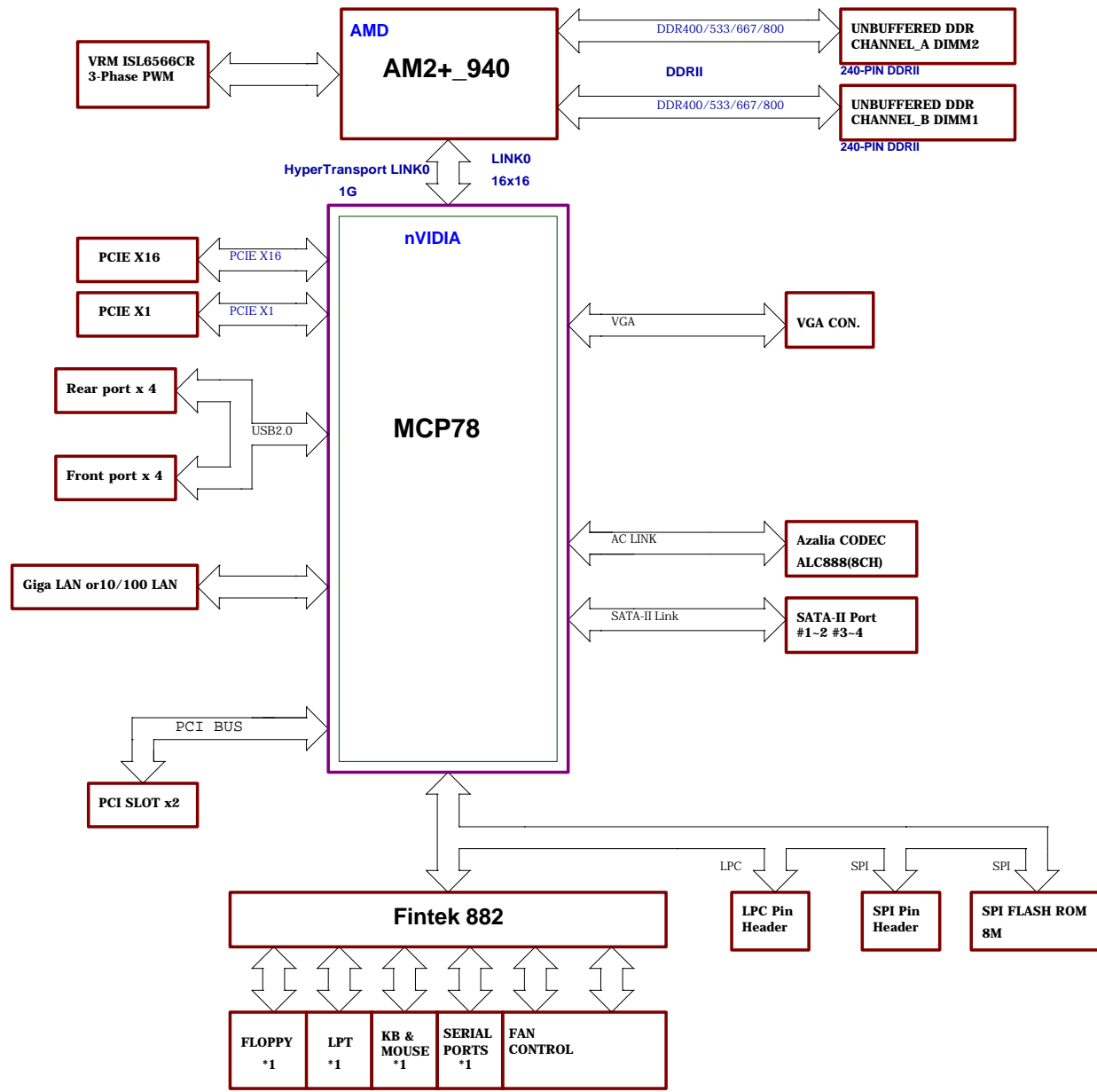
SATA(SATA2-300MB/s) * 4

USB2.0 *8 (Rear*4 Front*4)

COM PORT *1

LPT PORT *1

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CPU: AM2+	6,7,8,9
DDR2 DIMM(Dual Channel)	10,11,12
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LAN_ RTL8211BL/8201CL	20
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DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2 CH-A	10100000B	MEM_MAO_CLK_H0/L0 MEM_MAO_CLK_H1/L1 MEM_MAO_CLK_H2/L2
DIMM 1 CH-B	10100001B	MEM_MBO_CLK_H0/L0 MEM_MBO_CLK_H1/L1 MEM_MBO_CLK_H2/L2

PCI Config.

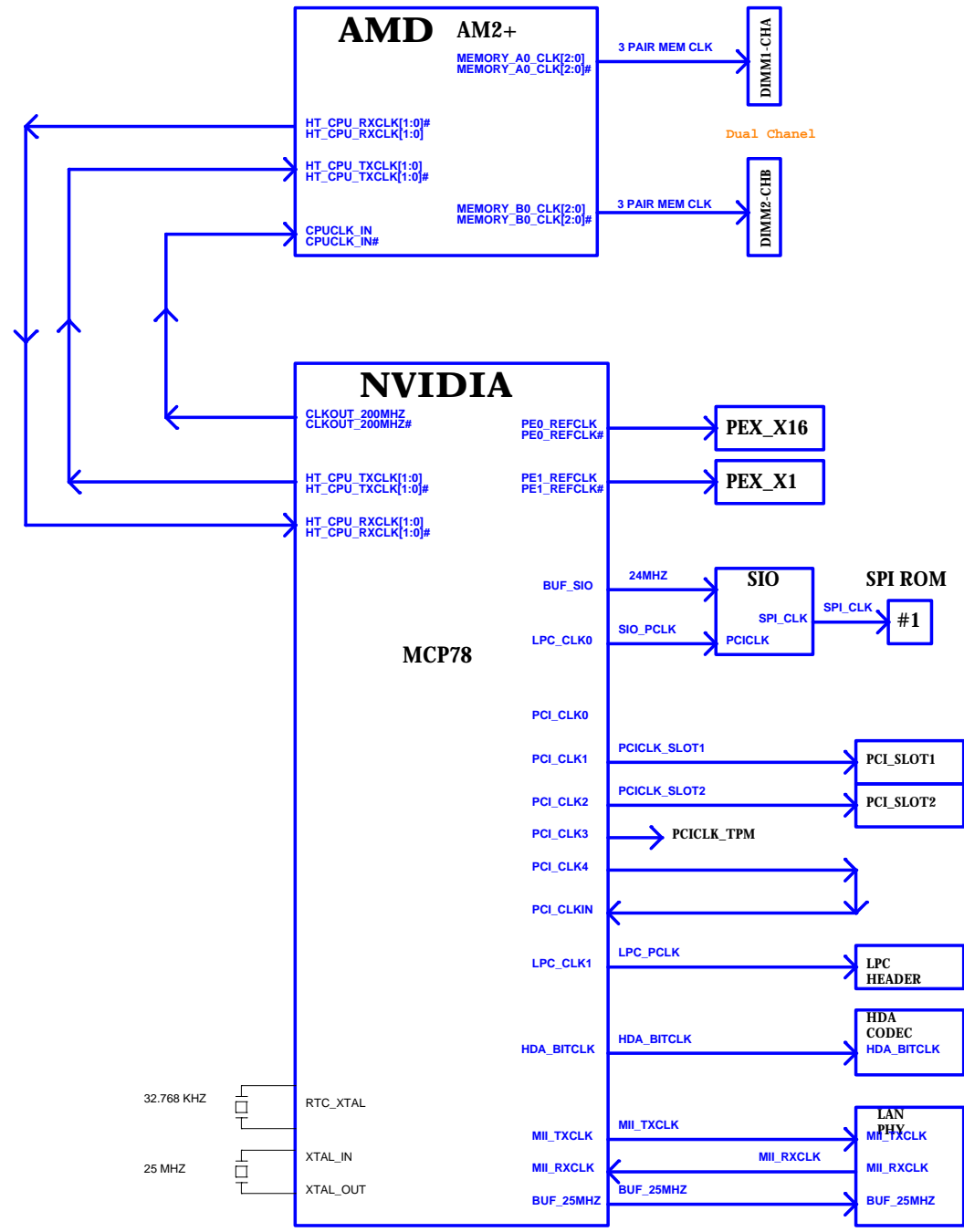
DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 2	PCI_INT#X PCI_INT#Y PCI_INT#Z PCI_INT#W	PCI_REQ4# PCI_GNT4#	AD25	PCI_CLKSLOT1 (PCICLK1)
PCI Slot 1	PCI_INT#W PCI_INT#X PCI_INT#Y PCI_INT#Z	PCI_REQ3# PCI_GNT3#	AD24	PCI_CLKSLOT2 (PCICLK2)
IEEE1394				PCIE2_CLK /PCIE2_CLK#
TPM				PCICLK_TPM (PCICLK3)
Chipset				PCI_CLKIN (PCICLK4)
LPC				LPC_PCLK
SIO				SIO_PCLK

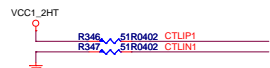
CPU VID TABLE	
VID	VOLTAGE
00000	1.5500V
00001	1.5250V
00010	1.5000V
00011	1.4750V
00100	1.4500V
00101	1.4250V
00110	1.4000V
00111	1.3750V
01000	1.3500V
01001	1.3250V
01010	1.3000V
01011	1.2750V
01100	1.2500V
01101	1.2250V
01110	1.2000V
01111	1.1750V
10000	1.1500V
10001	1.1250V
10010	1.1000V
10011	1.0750V
10100	1.0500V
10101	1.0250V
10110	1.0000V
10111	0.9750V
11000	0.9500V
11001	0.9250V
11010	0.9000V
11011	0.8750V
11100	0.8500V
11101	0.8250V
11110	0.8000V
11111	0.7750V

USB	Port	DATA +/ -	OC#
Rear	LAN_USB1	USB0- USB0+ USB1- USB1+	OC#0
	I1394_USB1	USB2- USB2+ USB3- USB3+	OC#1
Front	JUSB1	USB4- USB4+ USB5- USB5+	OC#2
	JUSB2	USB6- USB6+ USB7- USB7+	OC#3
		USB8- USB8+ USB9- USB9+	OC#4
		USB10- USB10+ USB11- USB11+	

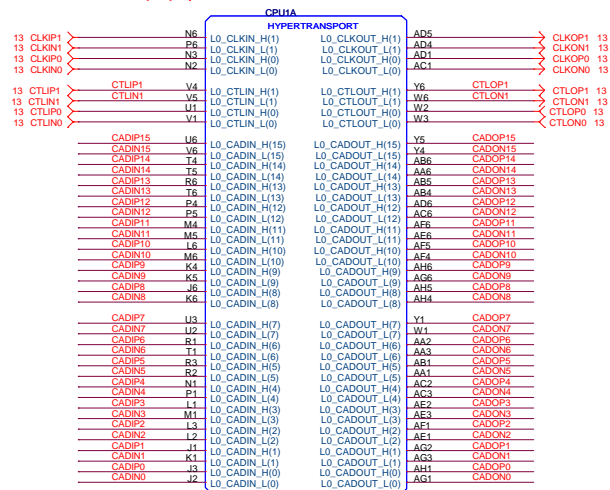
PCI RESET DEVICE

MCP61P , MCP68 , MCP78	
Signals	Target
PCI_RESET0*	PCISLOT1
PCI_RESET1*	PCISLOT2
PCI_RESET2*	MS6
PCI_RESET3*	1394
LPC_RESET*	LPC/SIO

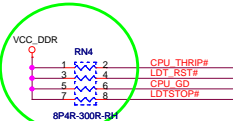




13 CADIP0..15] > CADIP0..15]
 13 CADIN0..15] > CADIN0..15]
 13 CADOP0..15] > CADOP0..15]
 13 CADON0..15] > CADON0..15]

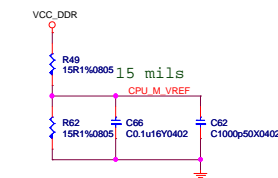


N12-9400050-F02

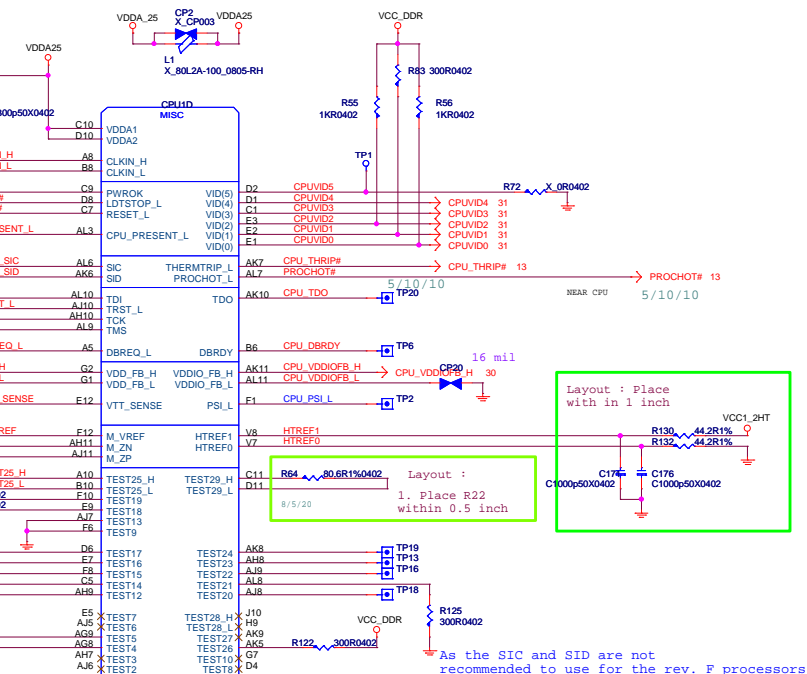
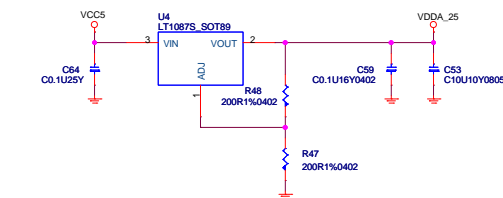


Layout : Place R63 within 0.5 inch of CPU

If SI is not used, the SID pin can be left unconnector and SIC should have a 300 ohm pulldown to VSS



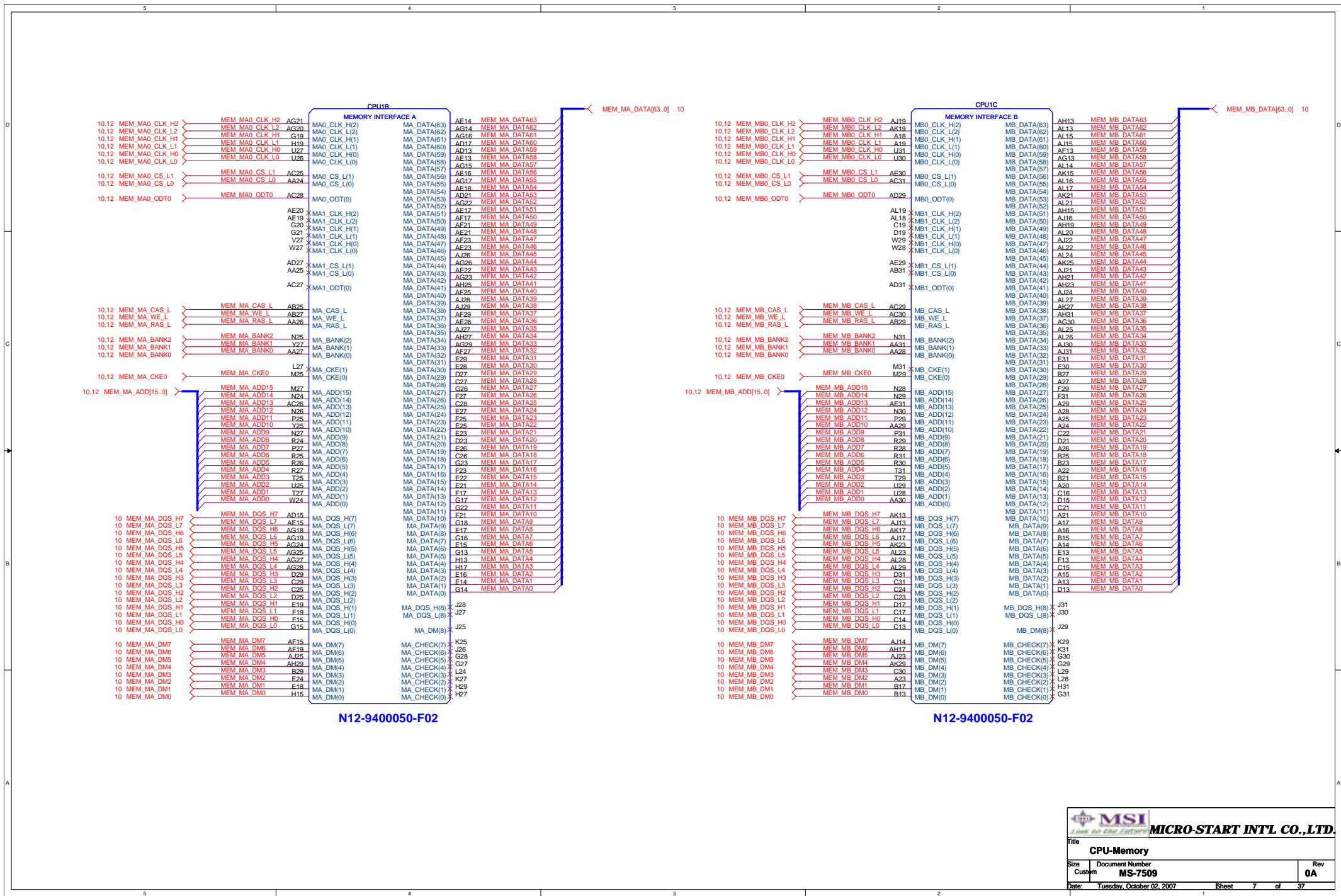
27 THERMDC_CPU
 27 THERMDA_CPU

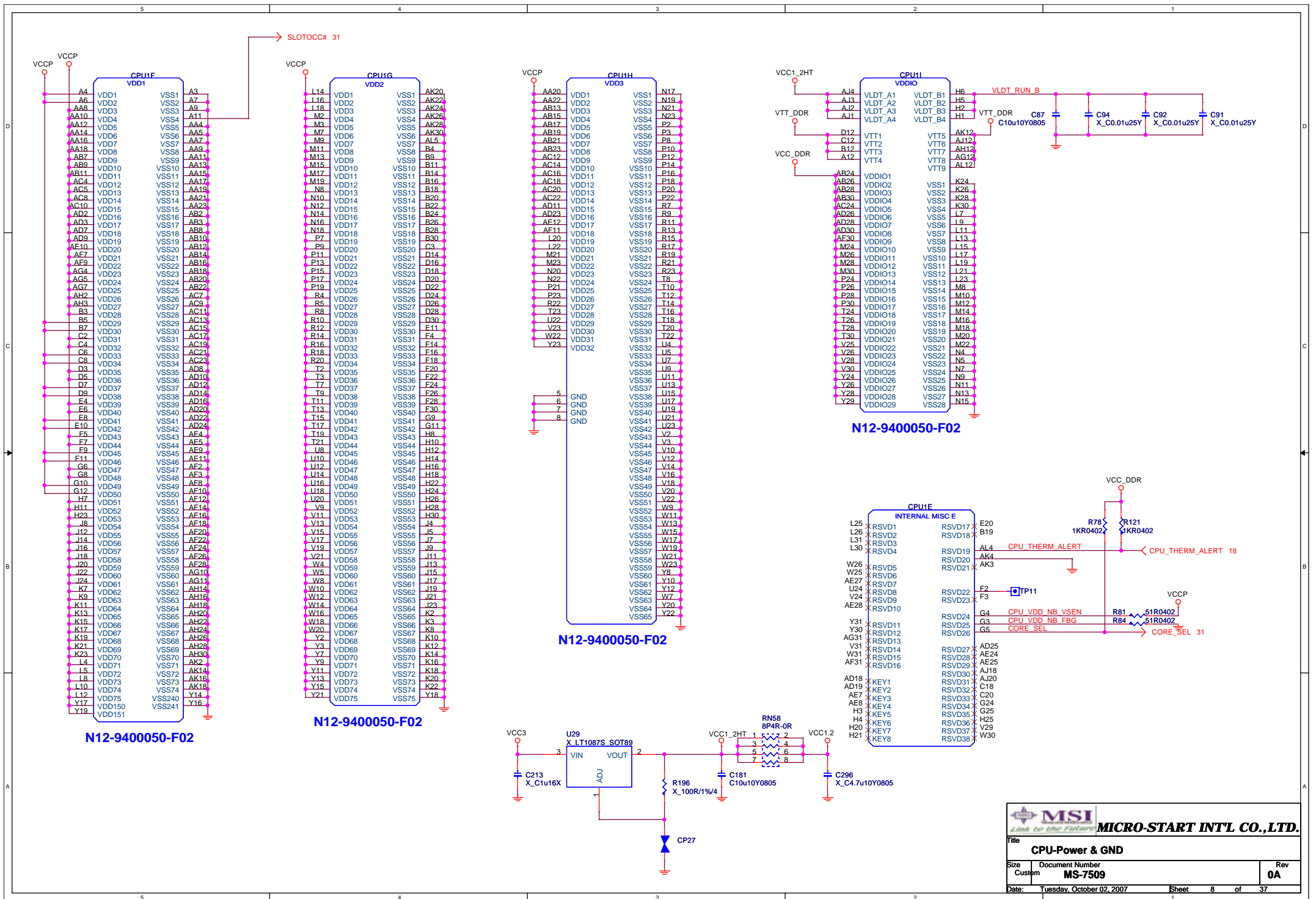


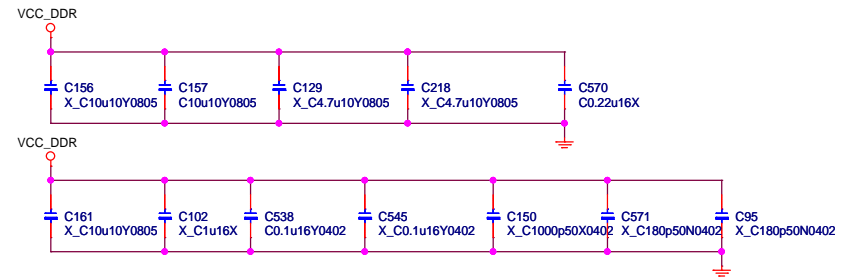
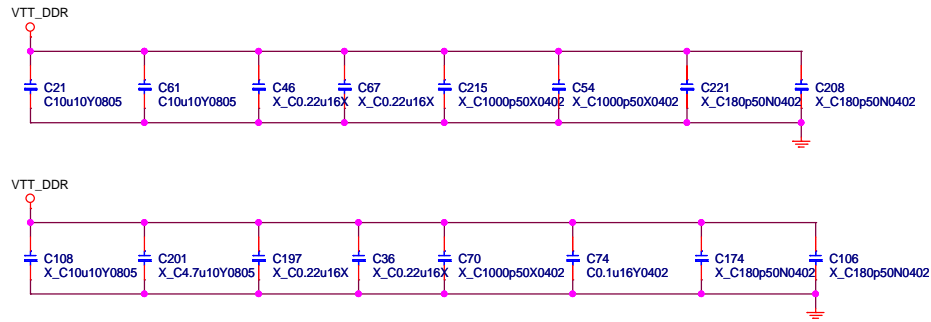
N12-9400050-F02

Layout : Place R22 within 0.5 inch

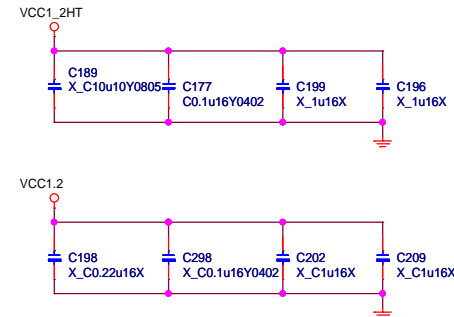
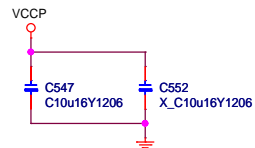
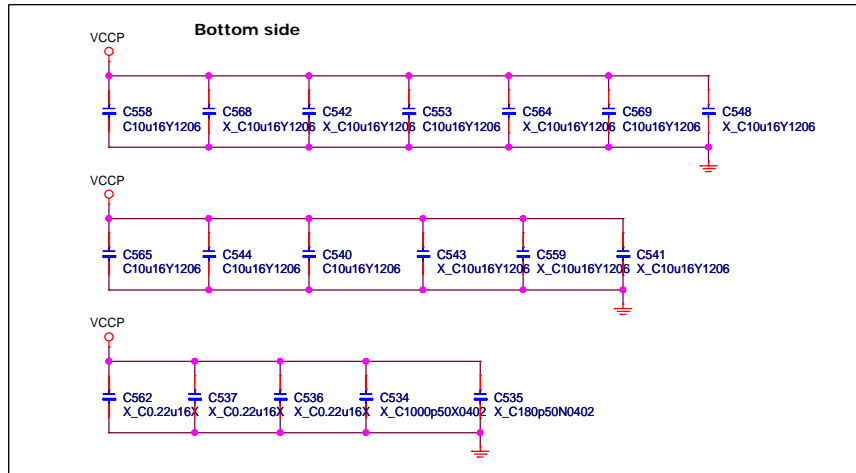
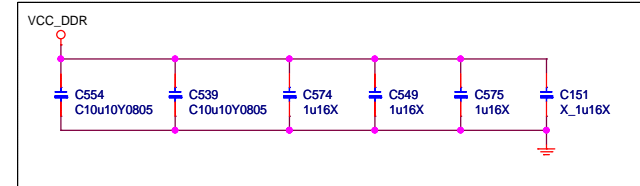
As the SIC and SID are not recommended to use for the rev. F processors.
 for NV Stuff R557 , R559
 for SIO Stuff R558 , R560

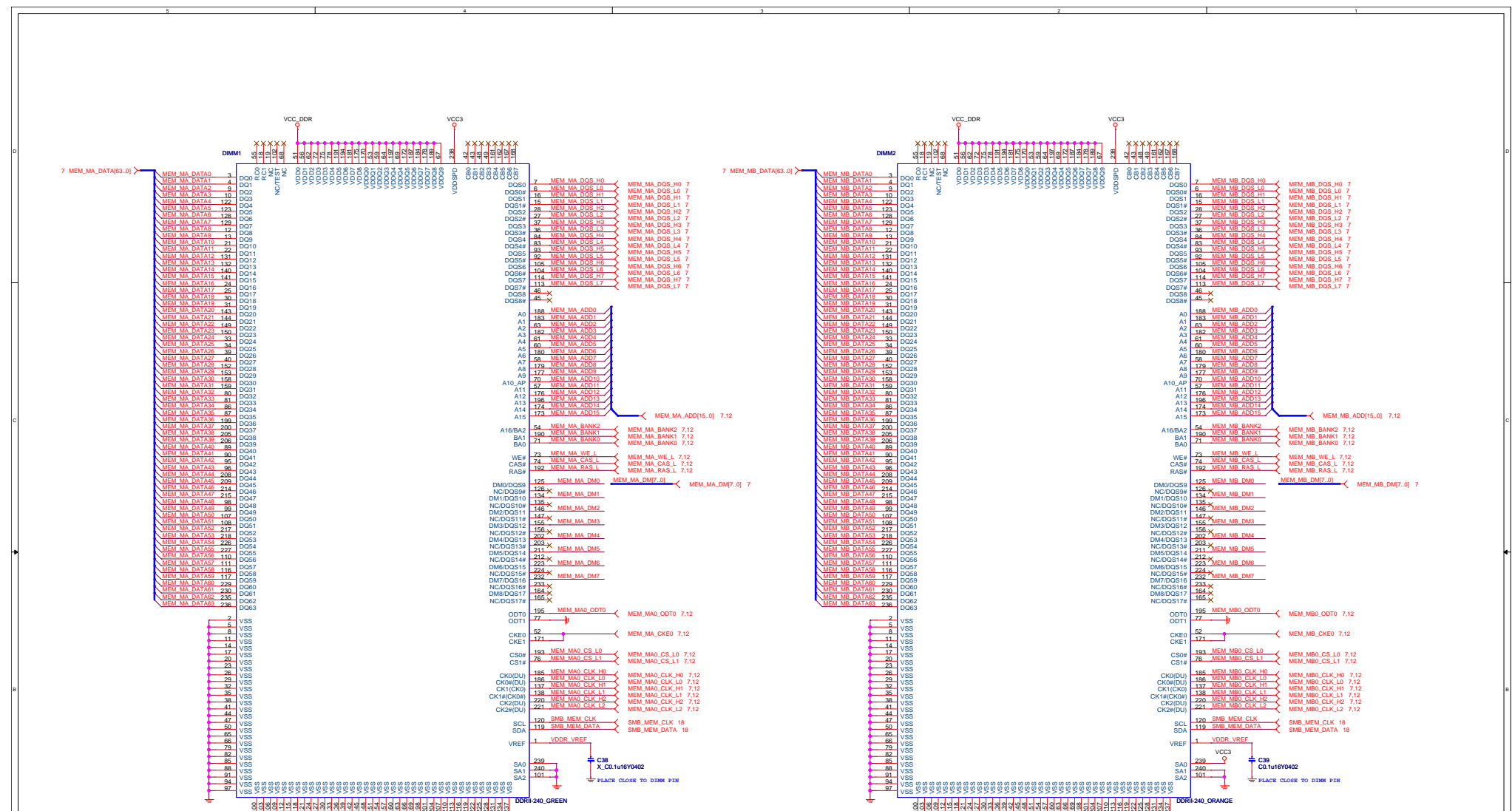




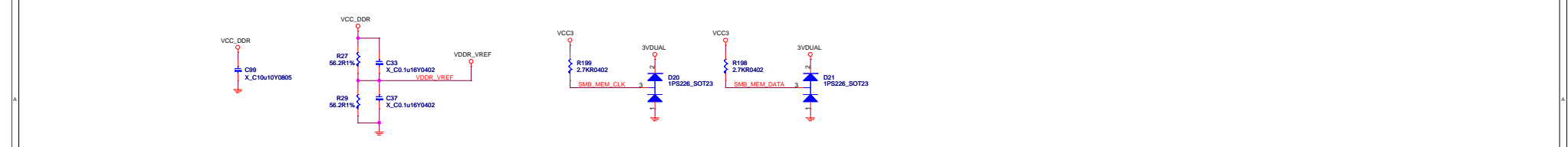


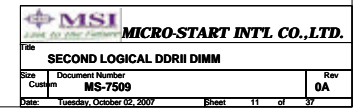
Bottom side



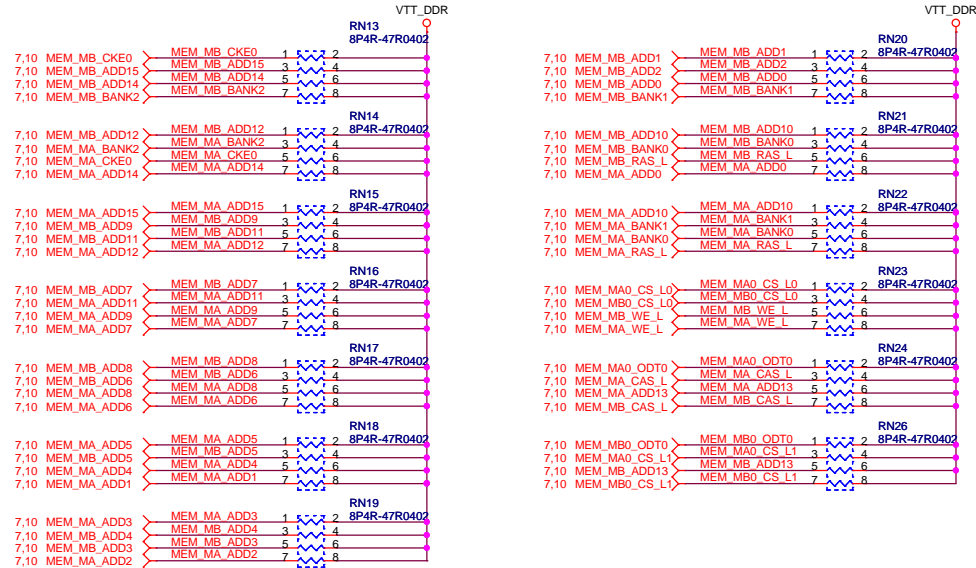


N13-2400301-K06 ADDRESS: 1010 000 N13-2400351-K06 ADDRESS: 1010 001

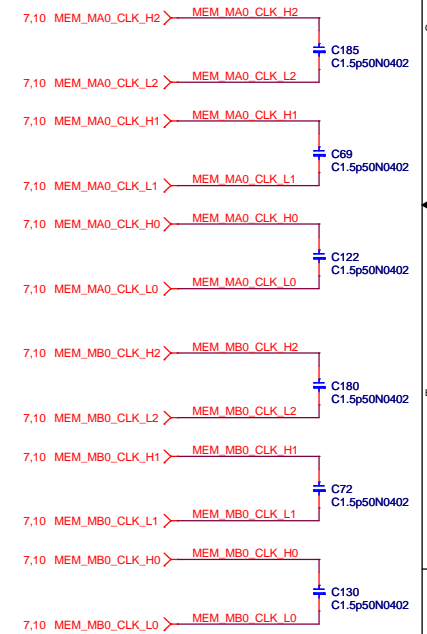
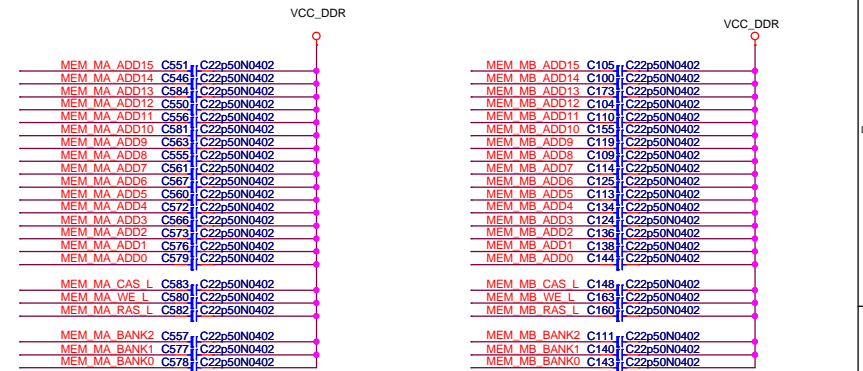




RTT:Place Behind DIMMs



Place Between Processor and DIMMs



MCP68 HyperTransport Receive

Connect directly to CPU HT Transmit Data Bus

CADOP[0..7] P/I N CADOP[8..15] P/I N
CTLOP0 P/I N CTLOP1 P/I N
CLKOP0 P/I N CLKOP1 P/I N

Breakout (<700 mil):

Route signal at nominal impedance and 1x trace width spacing.

After Breakout:

Route signal at the impedance specified in AMD Processor Motherboard Design Guide and 4x trace width spacing to other signals.

Match pairs to 25 mil.

All signal lengths must match to within 60 mil of

Minimum Length: 1" (150ps)

Maximum Length: 12" (1800ps) for trace ≥ 5mil and 8" (1200ps) for trace = 4mil

MCP68 HyperTransport Transmit

Connect directly to CPU HT Transmit Data Bus

CADIP[0..7] P/I N CADIP[8..15] P/I N
CTLIP0 P/I N CTLIP1 P/I N
CLKIP0 P/I N CLKIP1 P/I N

Breakout (<700 mil):

Route signal at nominal impedance and 1x trace width spacing.

After Breakout:

Route signal at the impedance specified in AMD Processor Motherboard Design Guide and 4x trace width spacing to other signals.

Match pairs to 25 mil.

All signal lengths must match to within 60 mil of

Minimum Length: 1" (150ps)

Maximum Length: 12" (1800ps) for trace ≥ 5mil and 8" (1200ps) for trace = 4mil

NF-6100-430-N-A2 (MCP61P) : B01-MCP6135-N08

NF-7050-630A-A1 (MCP68) : B01-MCP6805-N08

U14A
PBG692

MCP61
SEC 1 OF 8

6 CADOP[0..15] > CADOP[0..15]

6 CADON[0..15] > CADON[0..15]

6 CLKOP0 > CLKOP0
6 CLKON0 > CLKON0
6 CLKOP1 > CLKOP1
6 CLKON1 > CLKON1

6 CTLOP0 > CTLOP0
6 CTLO0 > CTLO0
6 CTLOP1 > CTLOP1
6 CTLO1 > CTLO1

VCC1.2

R150 150R1%0402

R338 150R1%0402

R39, R52

Within 600 mils of MCP68

PROCHOT#

CPU_THRIP#

5/10/10

VCC1.2

CP3

width 12 mil

1.2V_PLL_CPU_HT

70

1.2V_PLL_CPU_HT

1.2V_PLL_CPU

1.2

AC15

AB15

+1.2V_PLL_CPU_HT

+3.3V_PLL_CPU

<PATH>

PIN AB15 MCP68 = 3.3V/MCP78=1.1V

Solder Side

HyperTransport Calibration

HT_MCP_COMP_VDD

HT_MCP_COMP_GND

Breakout (<500 mil):

Route signal at nominal impedance

and 1x trace width spacing.

After Breakout:

Route signal at nominal impedance

and 2x (or greater) trace width spacing

Maximum Length: 600 mil.

MCP HyperTransport

HT_MCP_REQ# / -LDTSTOP

-LDT_RST / CPU_GD

Breakout (<700 mil):

Route signal at nominal impedance

and 1x trace width spacing.

After Breakout:

Route signal at nominal impedance

and 2x trace width spacing.

HT_MCP_TXD0_P AH23 CADIP0
HT_MCP_TXD1_P AH22 CADIP1
HT_MCP_TXD2_P AJ21 CADIP2
HT_MCP_TXD3_P AH21 CADIP3
HT_MCP_TXD4_P AH19 CADIP4
HT_MCP_TXD5_P AH18 CADIP5
HT_MCP_TXD6_P AJ17 CADIP6
HT_MCP_TXD7_P AH17 CADIP7
HT_MCP_TXD8_P AE22 CADIP8
HT_MCP_TXD9_P AB20 CADIP9
HT_MCP_TXD10_P AC20 CADIP10
HT_MCP_TXD11_P AE20 CADIP11
HT_MCP_TXD12_P AD18 CADIP12
HT_MCP_TXD13_P AE18 CADIP13
HT_MCP_TXD14_P AB17 CADIP14
HT_MCP_TXD15_P AC16 CADIP15

HT_MCP_TXD0_N AJ23 CADIN0
HT_MCP_TXD1_N AJ22 CADIN1
HT_MCP_TXD2_N AK21 CADIN2
HT_MCP_TXD3_N AG21 CADIN3
HT_MCP_TXD4_N AJ19 CADIN4
HT_MCP_TXD5_N AJ18 CADIN5
HT_MCP_TXD6_N AK17 CADIN6
HT_MCP_TXD7_N AG17 CADIN7
HT_MCP_TXD8_N AG22 CADIN8
HT_MCP_TXD9_N AB19 CADIN9
HT_MCP_TXD10_N AD20 CADIN10
HT_MCP_TXD11_N AF20 CADIN11
HT_MCP_TXD12_N AE18 CADIN12
HT_MCP_TXD13_N AG18 CADIN13
HT_MCP_TXD14_N AB16 CADIN14
HT_MCP_TXD15_N AD16 CADIN15

HT_MCP_TX_CLK0_P AH20 CLKIP0
HT_MCP_TX_CLK1_P AG20 CLKIN0
HT_MCP_TX_CLK1_N AB18 CLKIN1

HT_MCP_TXCTL0_P AH16 CTLIP0
HT_MCP_TXCTL0_N AG16 CTLO0
RESERVED AE16 CTLIP1
RESERVED AF16 CTLO1

HT_MCP_REQ# AH25 HT_MCP_REQ#
HT_MCP_STOP AH24 LDTSTOP#
HT_MCP_RST AG23 LDT_RST#
HT_MCP_PWRGD AG24 CPU_GD

CLKOUT_200MHZ_P AK25 CPUCLKO_H
CLKOUT_200MHZ_N AJ25 CPUCLKO_L

CPU_SBVREF AE24
CLKOUT_25MHZ AK26 CLKOUT25MHz

CLK200_TERM_GND AJ26

MCP68/A1/PBG692

MCP61P 2.37K
MCP68 NC
MCP78 2.37K

R44
Within 1000 mils of MCP68

HT_MCP_REQ# / -LDTSTOP

Route signal at nominal impedance

and 2x trace width spacing.

Maximum Length: 600 mil.

6 CADIP[0..15] > CADIP[0..15]

6 CADIN[0..15] > CADIN[0..15]

6 CLKIP0 > CLKIP0
6 CLKIN0 > CLKIN0
6 CLKIP1 > CLKIP1
6 CLKIN1 > CLKIN1

6 CTLIP0 > CTLIP0
6 CTLO0 > CTLO0
6 CTLIP1 > CTLIP1
6 CTLO1 > CTLO1

6 LDTSTOP# > LDTSTOP#
6 LDT_RST# > LDT_RST#
6 CPU_GD > CPU_GD

6 CPUCLKO_H > CPUCLKO_H
6 CPUCLKO_L > CPUCLKO_L

6 CLKOUT25MHz > CLKOUT25MHz

6 width 8 mil

6 5/10/10

6 MCP61P NC
6 MCP68 4.7u
6 MCP78 NC

6 Solder Side

6 VCC3 => 3VDUAL
6 GD => VCC3

6 R179 10KR0402

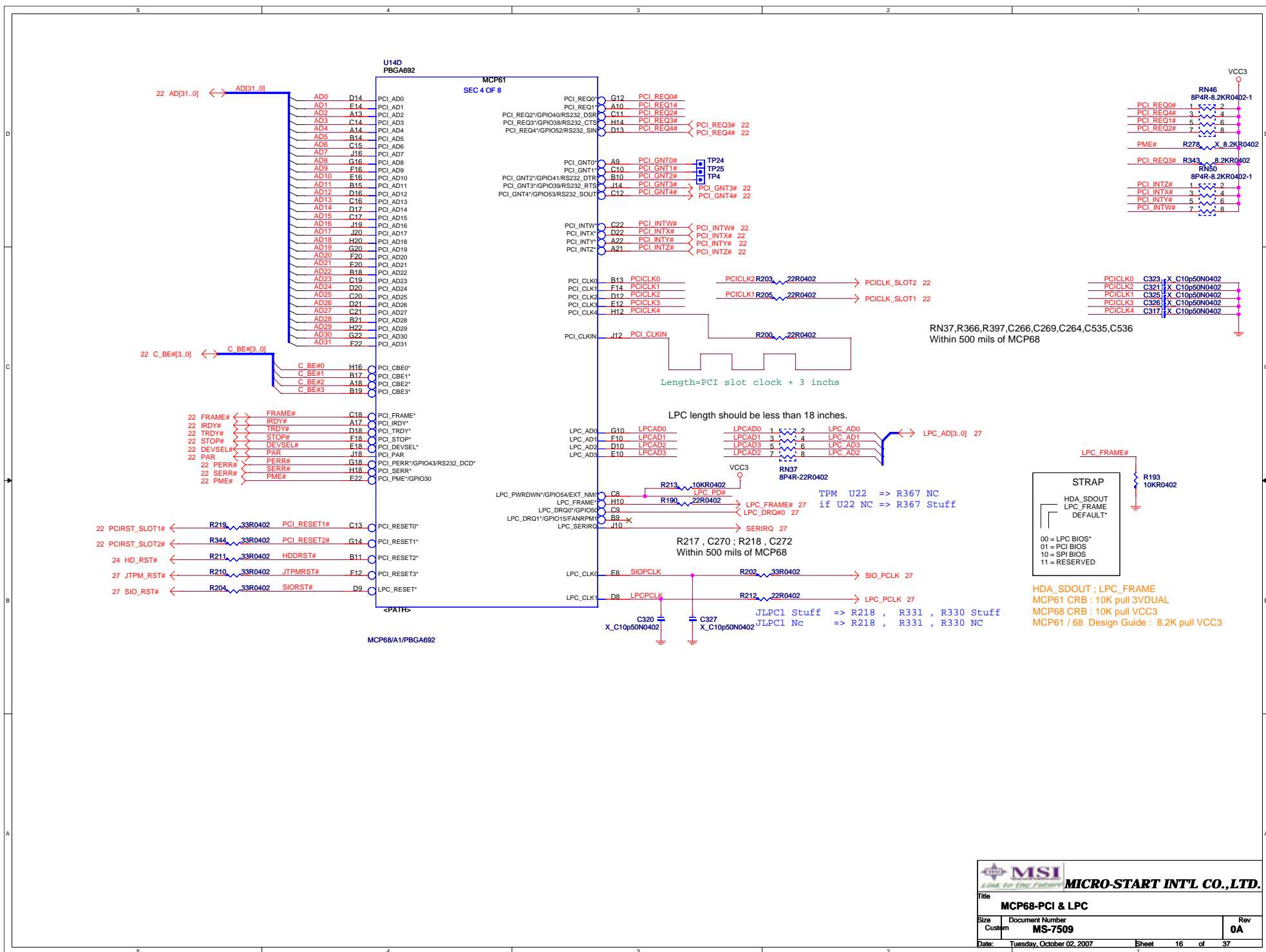
6 C179 Within 500 mils of MCP68

6 C244 C0.1u16V0402
6 C291 X_C4.7u10V0805



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Title MCP68-HT		
Size Custom	Document Number MS-7509	Rev 0A
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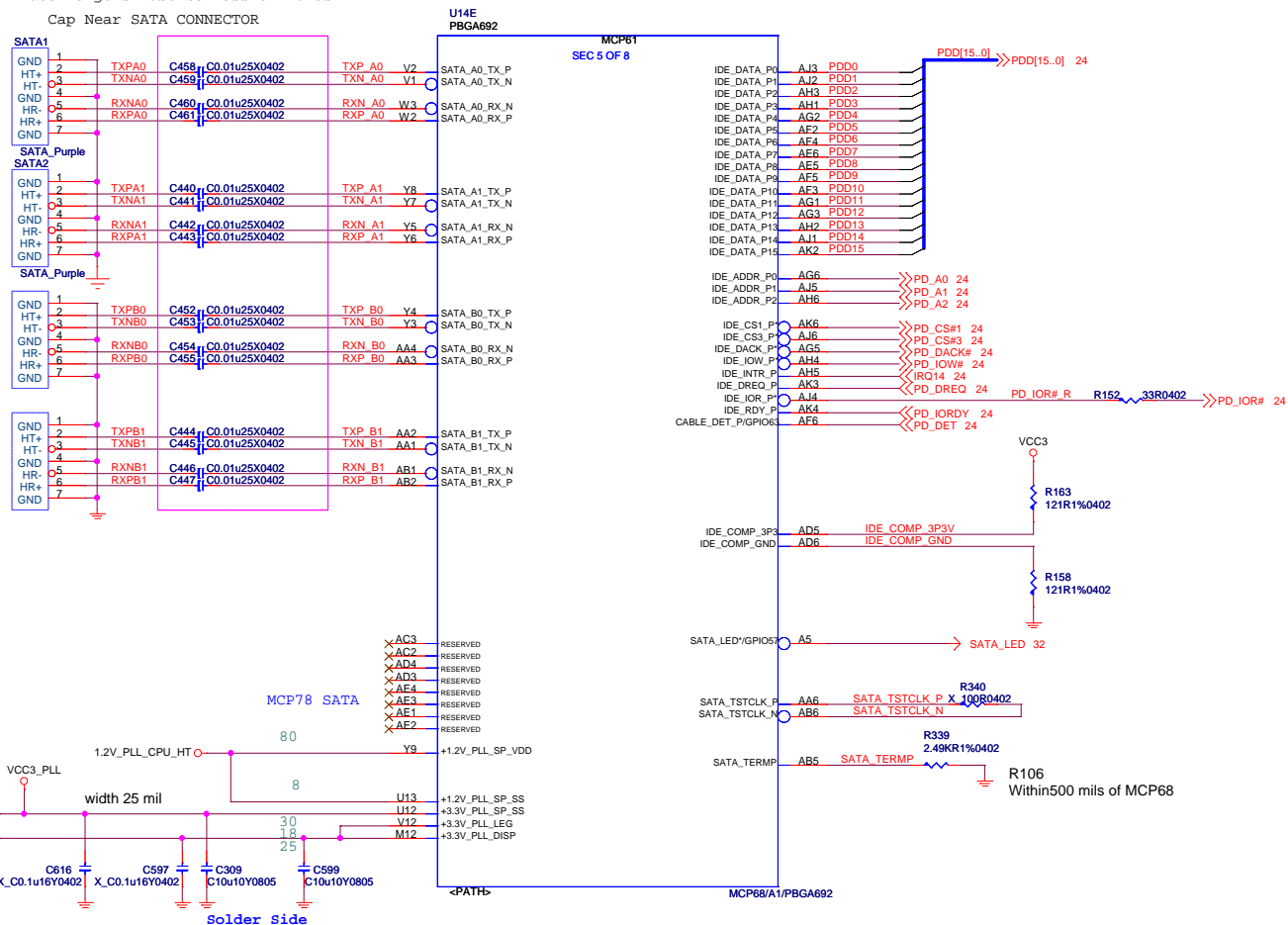


Trace lengths must be less 8 inches

Cap Near SATA CONNECTOR

N5N-07M0231-H06

MCP61P NC
MCP68 Stuff up
MCP78 Stuff up




Single-Ended Impedance

Trace Width (Based on 4-Layer Stackup)	Impedance	Interfaces
5 mil	60 Ω \pm 10%	All other interfaces
7 mil	50 Ω \pm 10%	RGMII, SATA
7.5 mil	45 Ω \pm 10%	USB

Differential Impedance

Trace Width (4-Layer Stackup)	Trace Spacing (4-Layer Stackup)	Impedance	Interfaces
5 mil	5 mil	93 Ω \pm 10%	HyperTransport
5 mil	6 mil	100 Ω \pm 10%	PCI Express
7 mil	12 mil	100 Ω \pm 10%	SATA
7.5 mil	7.5 mil	90 Ω \pm 10%	USB

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STRAP

HDA_SDOOUT
LPC_FRAME
DEFAULT*

00 = LPC BIOS*
01 = PCI BIOS
10 = SPI BIOS
11 = RESERVED

10KR0402

3VDUAL

R289
10KR0402

26 HDA_RST# ← HDA_RST#

HDA_RST#
1 = "RGMII"
0 = MII

R292
X_10KR0402

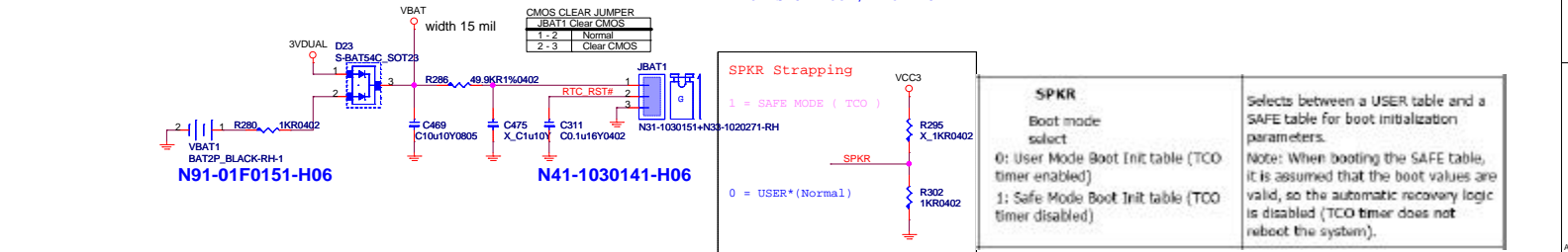
VCC3

R297
10KR0402

26 HDA_SYNC ← HDA_SYNC

HDA_SYNC
1 = "24MHZ
(SIO CLK)"
0 = 14.318MHZ
* = DEFAULT

R296
X_10KR0402



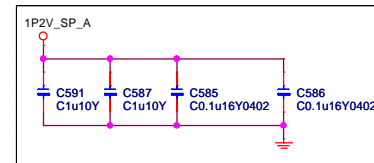
<p>SPKR</p> <p>Boot mode select</p> <p>0: User Mode Boot Init table (TCO timer enabled)</p> <p>1: Safe Mode Boot Init table (TCO timer disabled)</p>	<p>Selects between a USER table and a SAFE table for boot initialization parameters.</p> <p>Note: When booting the SAFE table, it is assumed that the boot values are valid, so the automatic recovery logic is disabled (TCO timer does not reboot the system).</p>
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MCP68

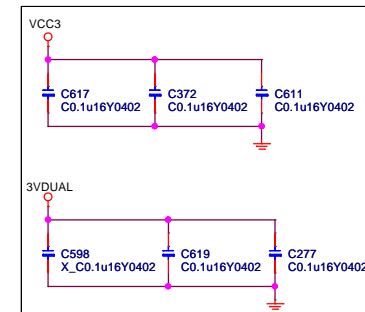
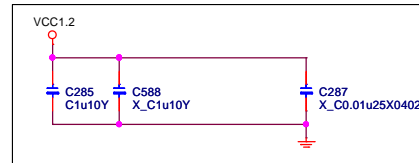
Preliminary Thermal Properties and Recommended Limits

Parameter	Value	Notes
Design ambient	43 °C	AMD max internal case temperature for CPU
Minimum Case to Ambient Solution	4.6 C/W	Assume 90% to heat sink and 10% to printed circuit board
TDP Max	13 W	Thermal Design Power (TDP) based on worst case process
Tcase Max	110 °C	Measured top center of chip without heat sink

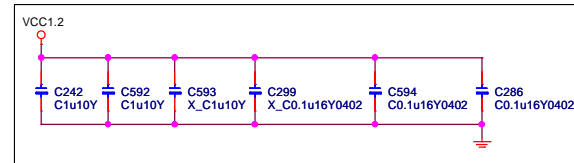
BACK SIDE



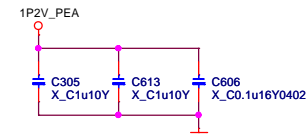
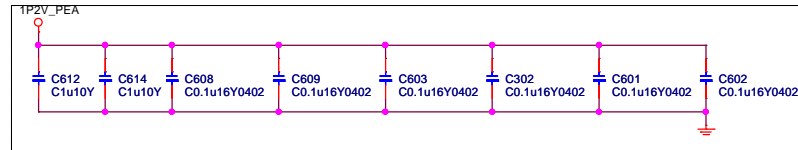
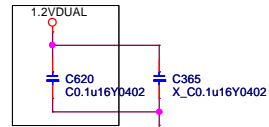
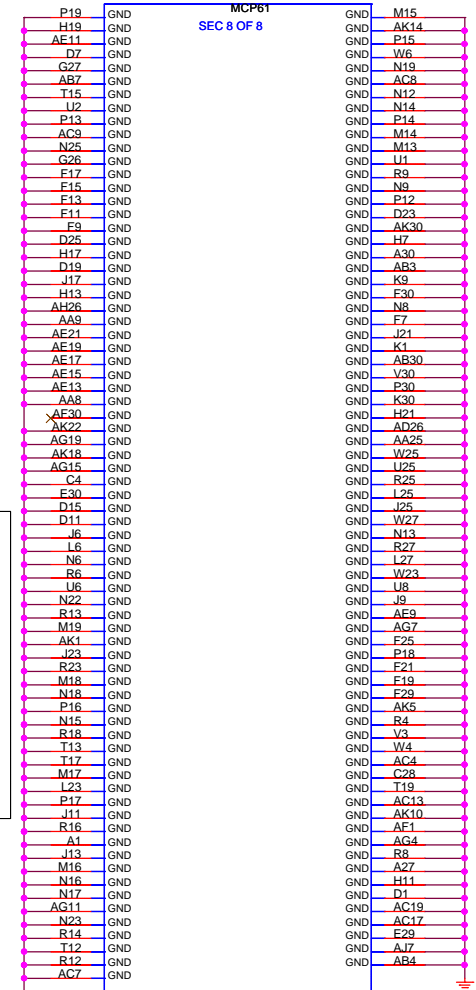
BACK SIDE

PLACE ON BACK SIDE
CENTER OF MCP68

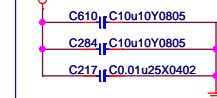
BACK SIDE



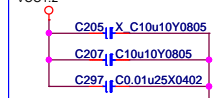
BACK SIDE

U14H
PBG692MCP61
SEC 8 OF 8

Place close to Q34

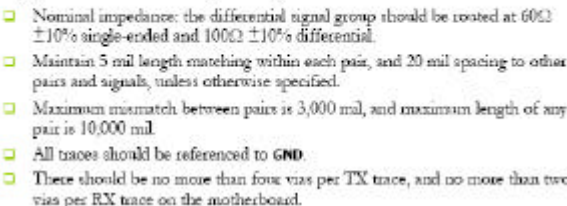


Place close to Q22

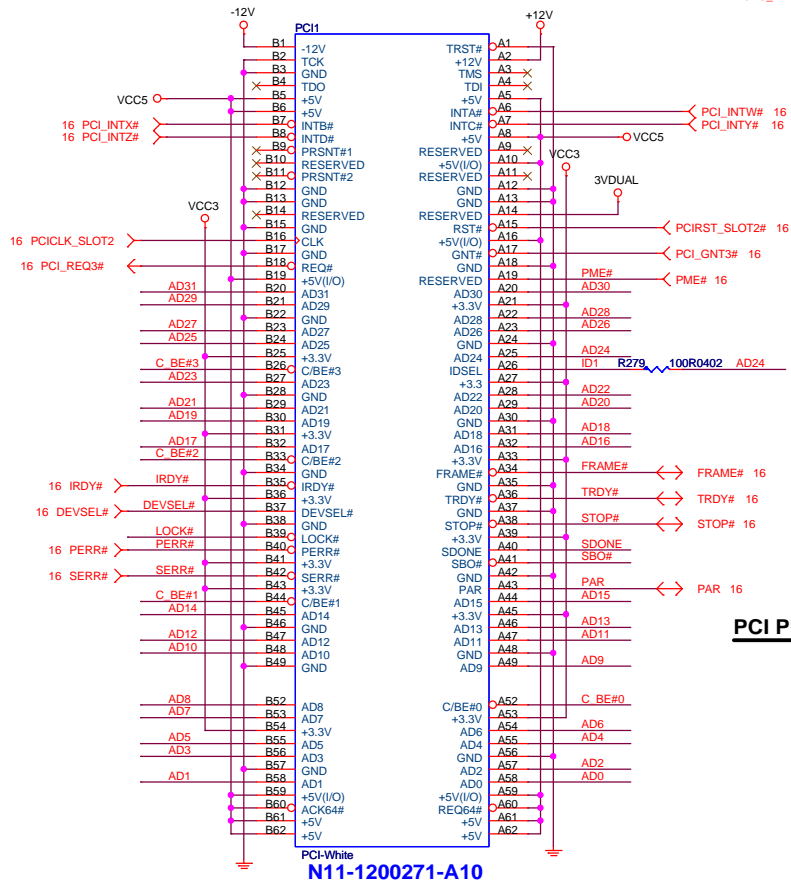


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Title MCP68-Power & GND			Rev 0A
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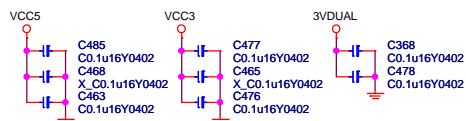


PCI SLOT 1 (PCI VER: 2.3 COMPLY)



MCP61P	MCP68
IDSEL = AD24	IDSEL = AD24
PCI_REQ2# PCI_GNT2#	PCI_REQ3# P
PCI_INTW#	PCI_INTW#
Device # 7	Device # 8

PCI SLOT DECOUPLING CAPACITORS



MCP61 IDSEL, INT, and REQ/GNT

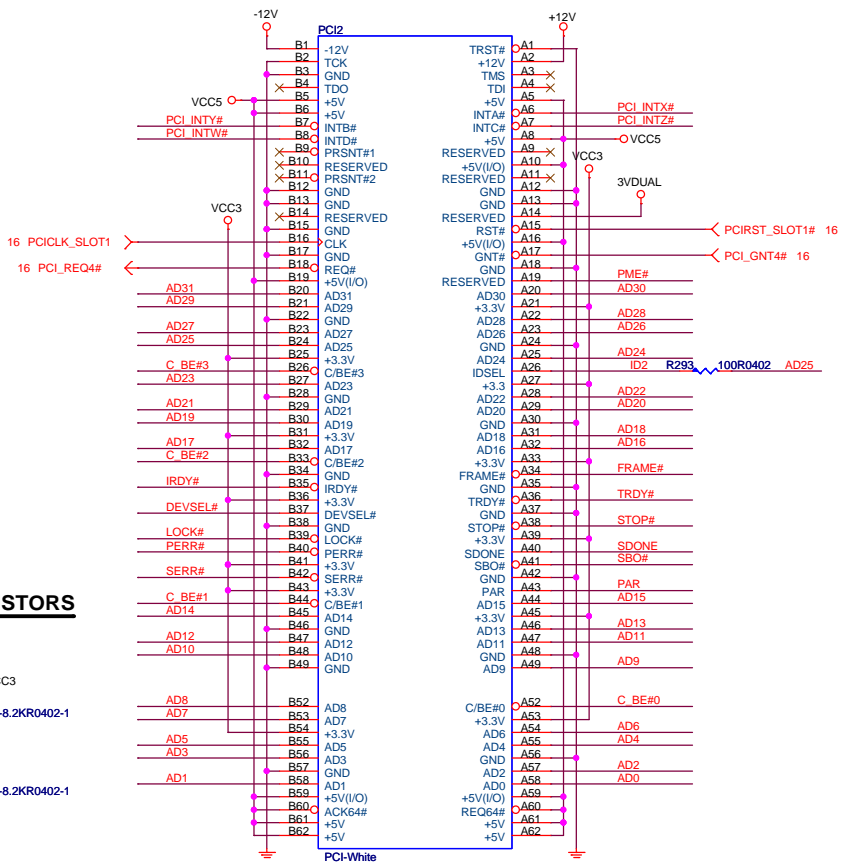
Slot	IDSEL	Slot INTA#	Slot INTB#	Slot INTC#	Slot INTD#	REQ/GNT	Device #
1	PCI_A025	INTA#	INTB#	INTC#	INTD#	4	5
2	PCI_A025	INTA#	INTC#	INTD#	INTB#	1	0
3	PCI_A024	INTA#	INTB#	INTD#	INTC#	2	7
4	PCI_A023	INTA#	INTB#	INTD#	INTC#	1	6
5	PCI_A022	INTA#	INTB#	INTC#	INTD#	0	5

MCP68 IDSEL, INT, and REQ/GNT

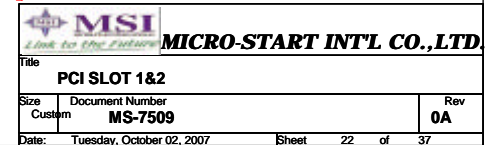
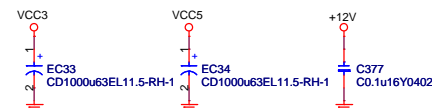
Slot	IDSEL	Slot INTA#	Slot INTB#
1	PCI_A025	INTx0	INTx0
2	PCI_A024	INTx#	INTx#
3	PCI_A023	INTz#	INTz#
4	PCI_A022	INTy#	INTy#
5	PCI_A021	INTx0	INTx0

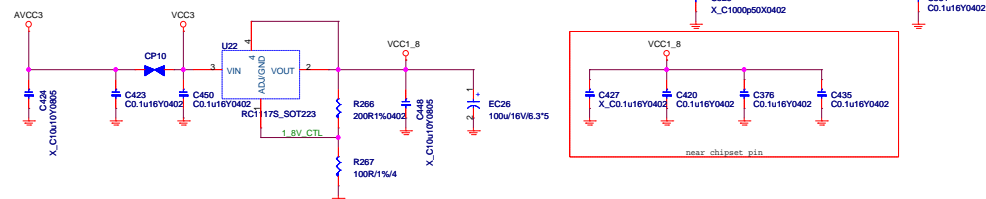
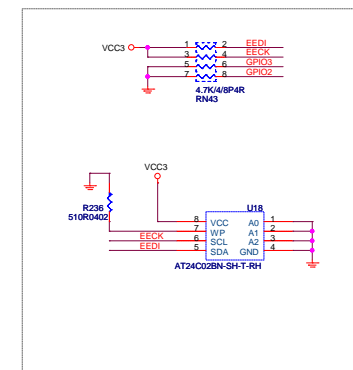
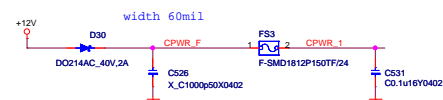
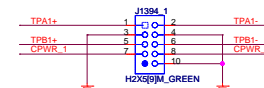
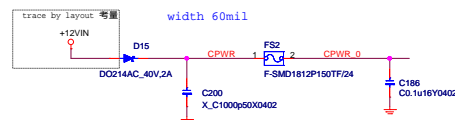
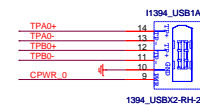
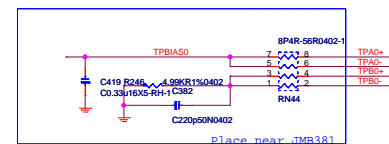
REQ/GNT	Device #
4	9
3	8
2	7
1	6
0	5

PCI SLOT 2 (PCI VER: 2.3 COMPLY)



MCP61P	MCP68	SDONE SBO#
IDSEL = AD25	IDSEL = AD25	
PCI_REQ3# PCI_GNT3#	PCI_REQ4# PCI_GNT4#	
PCI_INTX#	PCI_INTX#	
Device # 8	Device # 9	



Rear 1394 port

The schematic diagram illustrates the PD07 module and its connections. At the top left, a VCC5 supply is connected to pin 1 of the PD07 module via a resistor R220 (X_510R0402). The PD07 module is represented by a large blue rectangle with pins numbered 1 through 32. To the right of the module, a table lists the pin numbers and their corresponding functions:

Pin	Function
1	PD07
2	PD08
3	PD06
4	PD09
5	PD05
6	PD10
7	PD04
8	PD11
9	PD03
10	PD12
11	PD02
12	PD13
13	PD01
14	PD14
15	PD15
16	
17	
18	
19	
20	
21	
22	
23	
24	
25	
26	
27	
28	
29	
30	
31	
32	

Control signals are connected to the module as follows:

- 16 HD_RST#** and **HD_RST#** are connected to pin 1.
- 17 PD_DREQ** is connected to pin 21.
- 17 PD_IOW#** is connected to pin 23.
- 17 PD_IOR#** is connected to pin 25.
- 17 PD_IORDY** is connected to pin 27.
- 17 PD_DACK#** is connected to pin 29.
- 17 IRQ14** is connected to pin 31.
- 17 PD_A1** is connected to pin 33.
- 17 PD_A0** is connected to pin 35.
- 17 PD_CS#1** is connected to pin 37.
- 32 PD_LED** is connected to pin 39.

Other components and connections include:

- A resistor **R156 (X_8.2KR0402)** is connected to VCC3 and pin 14 (IRQ14).
- Pin 17 (PD_DET) is connected to a signal line labeled **PD_DET**, which is also connected to pin 17 of the PD07 module.
- Pin 18 (PD_A2) is connected to a signal line labeled **PD_A2**, which is also connected to pin 18 of the PD07 module.
- Pin 19 (PD_CS#3) is connected to a signal line labeled **PD_CS#3**, which is also connected to pin 19 of the PD07 module.
- Pin 20 (PD07) is connected to a signal line labeled **PD07**, which is also connected to pin 20 of the PD07 module.
- A resistor **R221 (X_10KR0402)** is connected to VCC5 and pin 21.
- Pin 22 (PD08) is connected to a signal line labeled **PD08**, which is also connected to pin 22 of the PD07 module.
- Pin 23 (PD09) is connected to a signal line labeled **PD09**, which is also connected to pin 23 of the PD07 module.
- Pin 24 (PD10) is connected to a signal line labeled **PD10**, which is also connected to pin 24 of the PD07 module.
- Pin 25 (PD11) is connected to a signal line labeled **PD11**, which is also connected to pin 25 of the PD07 module.
- Pin 26 (PD12) is connected to a signal line labeled **PD12**, which is also connected to pin 26 of the PD07 module.
- Pin 27 (PD13) is connected to a signal line labeled **PD13**, which is also connected to pin 27 of the PD07 module.
- Pin 28 (PD14) is connected to a signal line labeled **PD14**, which is also connected to pin 28 of the PD07 module.
- Pin 29 (PD15) is connected to a signal line labeled **PD15**, which is also connected to pin 29 of the PD07 module.

27 CPU_FAN_CTL 1 CPU_FAN_CTL 2 CPU_FAN_S1 3 SYS_FAN_CTL 4 +12V

C228 Co.1u10F0402 C232 Co.1u10F0402

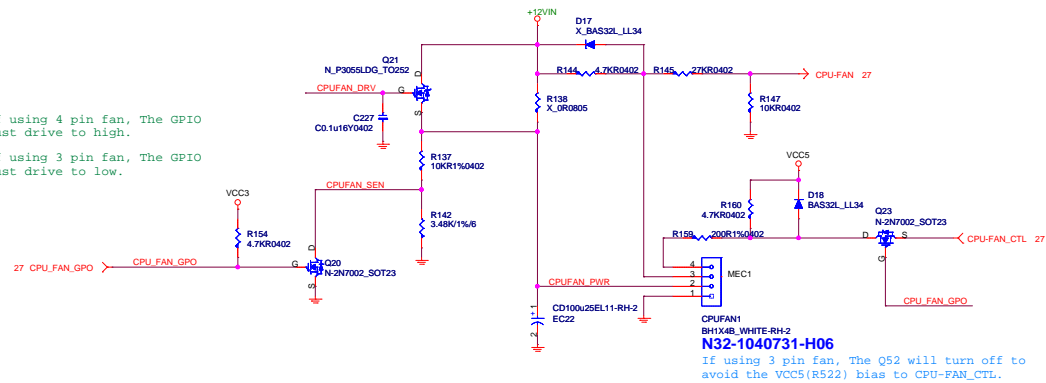
U15

1 FAN1_1 2 FAN2_1 3 VCC1_1 4 C1 5 FAN1_2 6 FAN2_2 7 FAN3_1 8 CHIRPMP GND 14 CPUFAN_DRV 13 CPUFAN_SEN 12 SYSFAN_DRV 11 SYSFAN_SEN

W83931TG

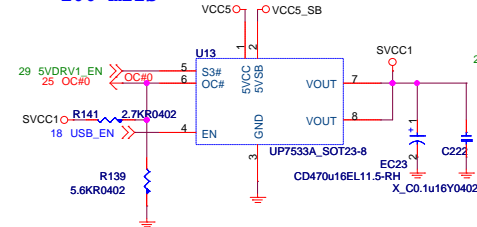
If using 4 pin fan,
must drive to high.

If using 3 pin fan,
must drive to low.

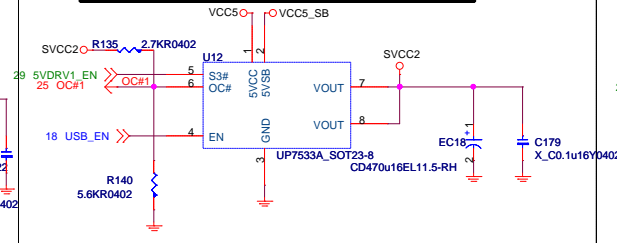


POWER CIRCUIT FOR USB PORT 0,1

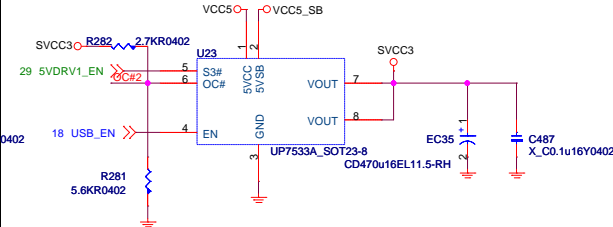
100 mils



POWER CIRCUIT FOR USB PORT 2,3

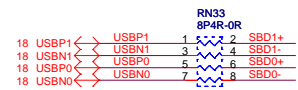


POWER CIRCUIT FOR USB PORT 4,5

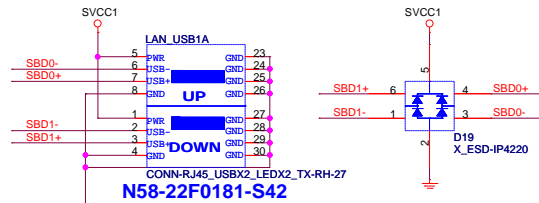


REAR PANEL USB CONNECTOR FOR USB PORT 0,1

Trace lengths must be less 12 inches



Match pairs to 50 mil.

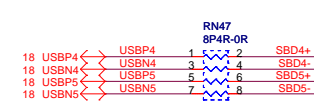


NEAR USB CONNECTOR

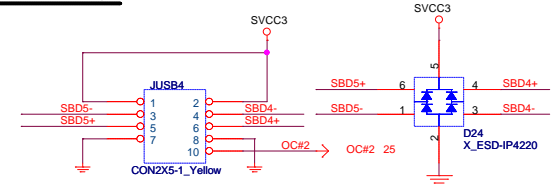
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

Trace lengths must be less 5 inches



Match pairs to 50 mil.

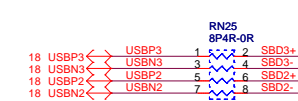


NEAR USB CONNECTOR

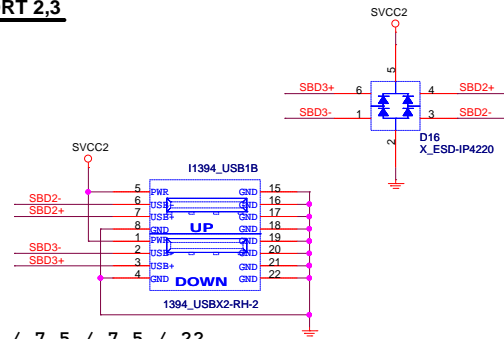
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

REAR PANEL USB CONNECTOR FOR USB PORT 2,3

Trace lengths must be less 12 inches



Match pairs to 50 mil.

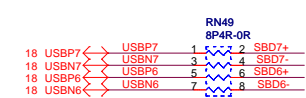


NEAR USB CONNECTOR

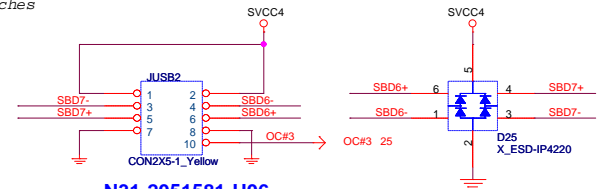
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

Trace lengths must be less 5 inches



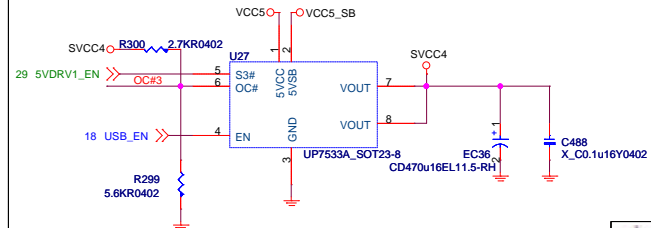
Match pairs to 50 mil.



NEAR USB CONNECTOR

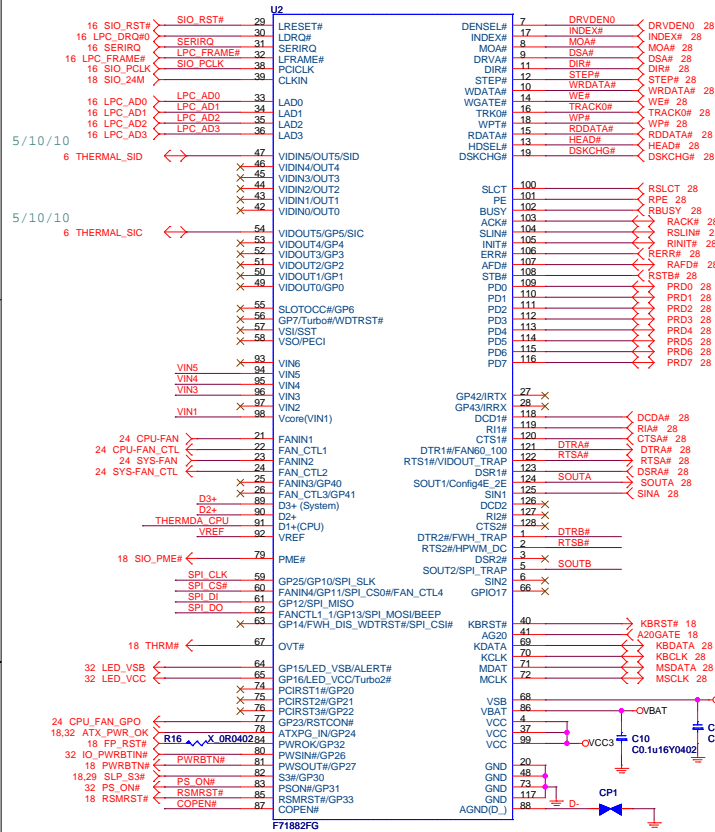
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

POWER CIRCUIT FOR USB PORT 6,7

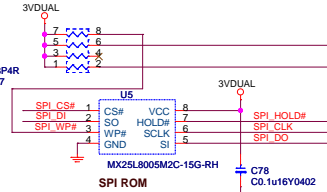
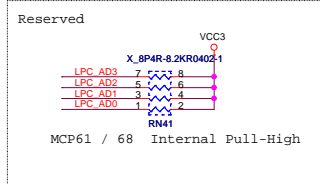
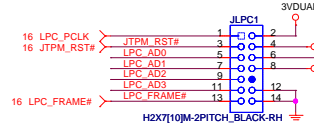


LPC SUPER I/O F71882

LPC length should be less than 18 inches.



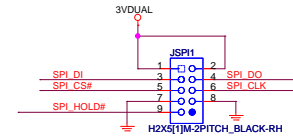
TPM PORT



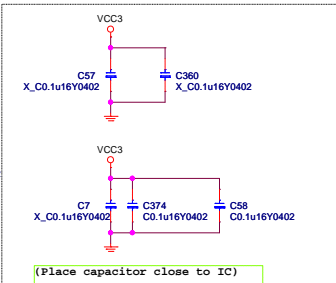
M31-25L8013-M24
M31-25X8003-W03

SPI DEBUG PORT

Place close to SPI ROM

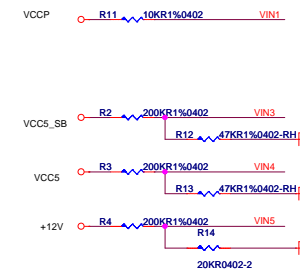


Part Number : N31-2051451-H06



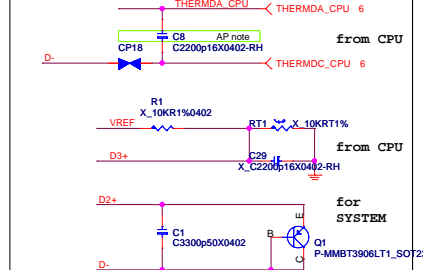
VOLTAGE SENSING (H/W Monitor).

The best voltage input level is about 1V.

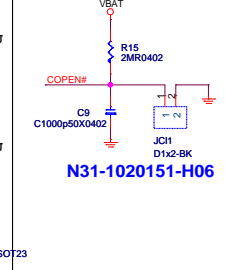


Temperature Sensing

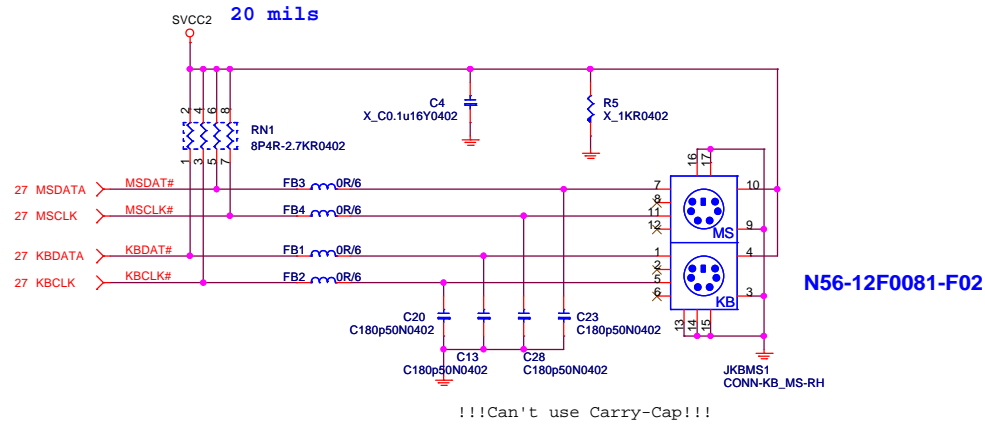
DIODE SENSING CIRCUIT



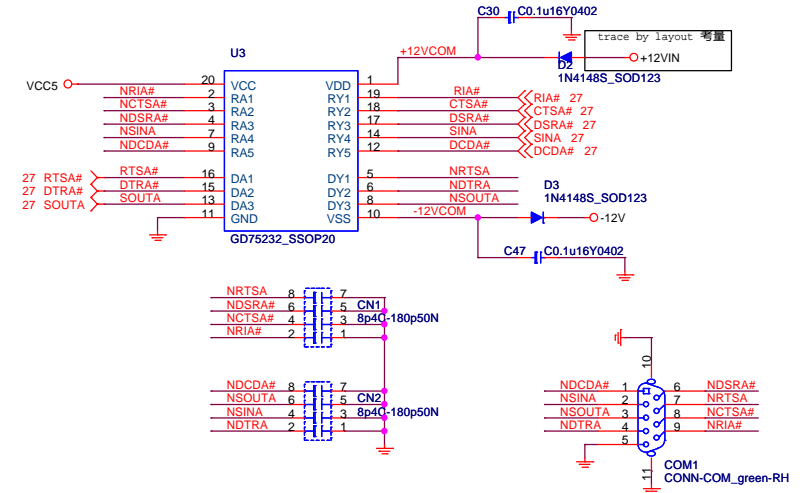
CASE OPEN CIRCUIT



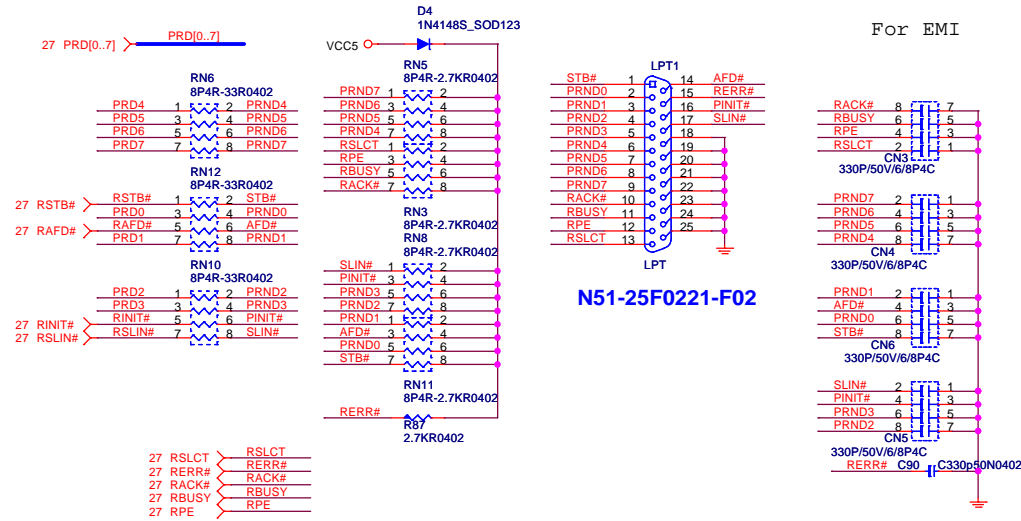
PS2 KEYBOARD & MOUSE CONNECTOR



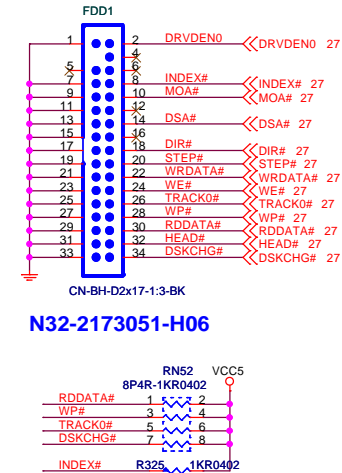
SERIAL PORT 1



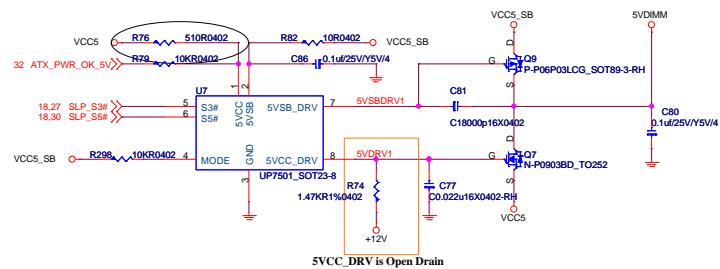
PARALLAL PORT



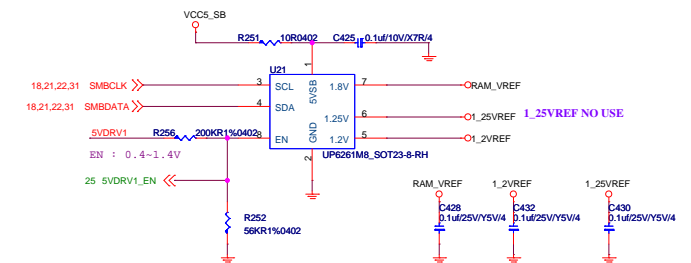
FLOPPY CONN BOLCK



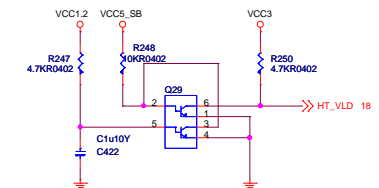
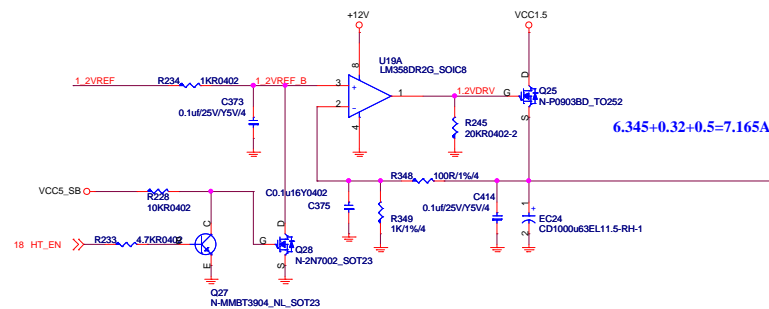
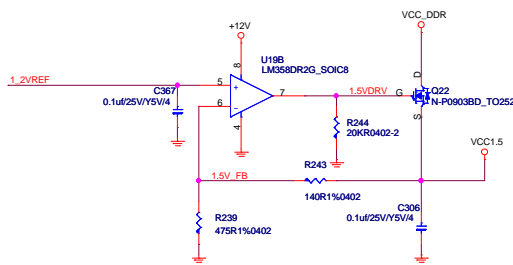
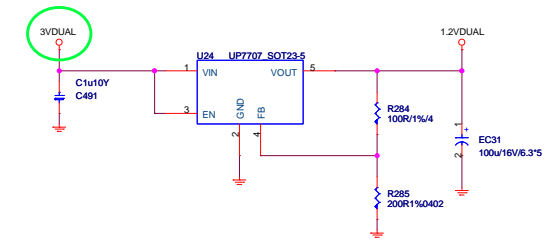
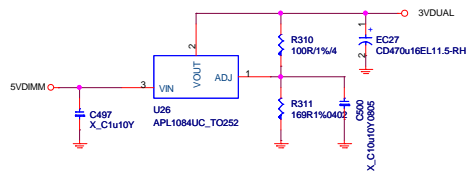
5V DIMM FOR DDR



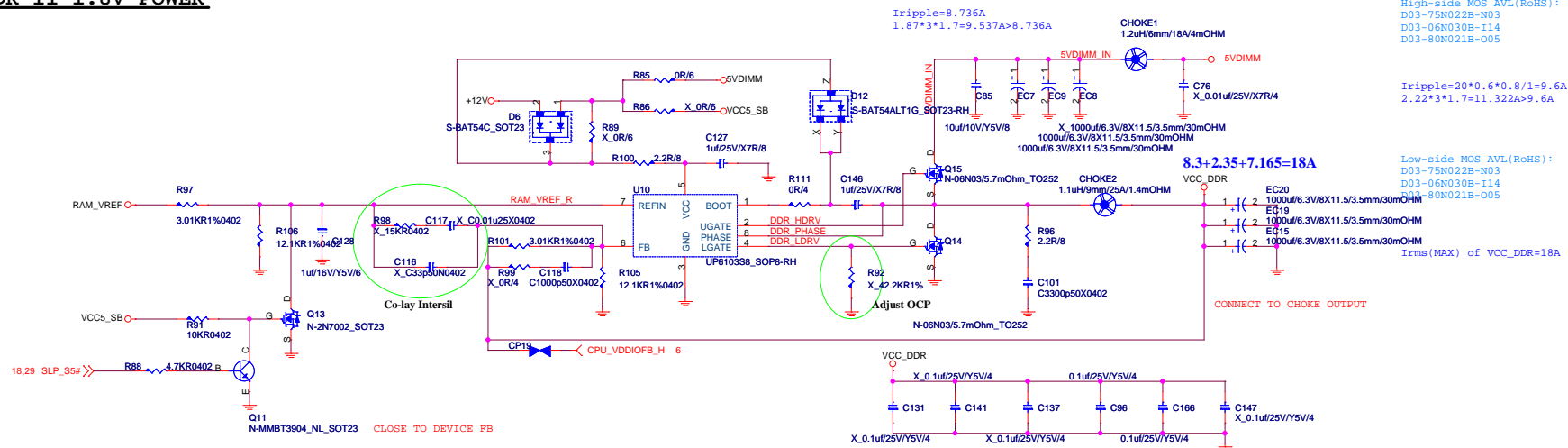
	S0	S3	S4	S5
DUAL_CTRL	X	X	0 1 1	0 1 1
5VSBDRV1	1	0	1 0 0	1 0 0
5VDRV1	1	0	0 0 0	0 0 0
5VSBDRV2	X	0	1 0 0	1 0 0
USB_EN	1	1	X 1 0	X 1 0
5VDIMM	Y	Y	N Y Y	N Y Y
USB power	Y	Y	N Y N	N Y N



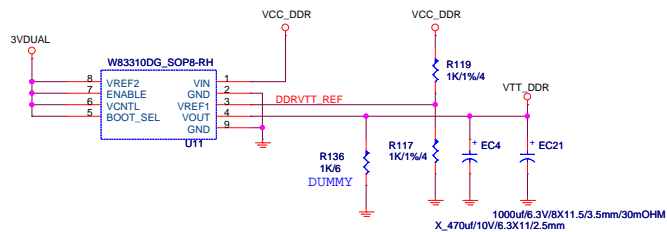
3VDUAL CONTROLLER



DDR II 1.8V POWER



DDR VTT Power



R389 NC ; R571 0 Ohm.
VCC1.2 from 1.2 ~ 1.5 Volt

VREF_SEL = 1.2V R352 => NC

$V_{out} = 1.25 \text{ Volt}$

Vout = 1.26 ~ 1.57 Volt

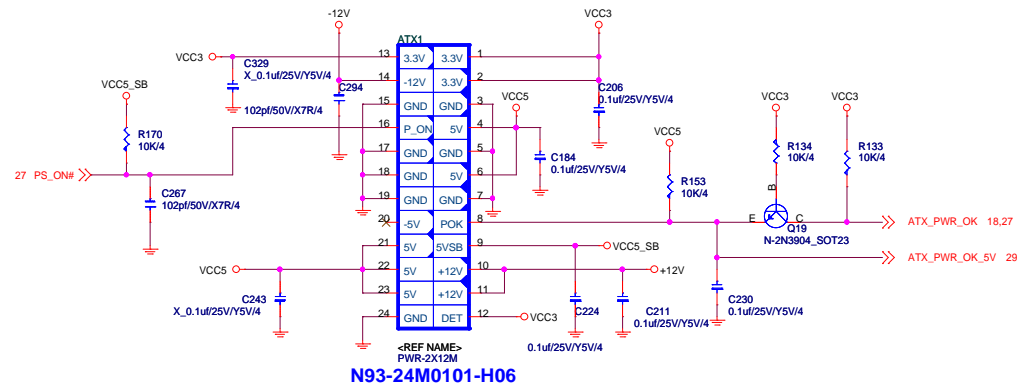
$$V_{out} = 1.2 \left[\left(\frac{49.9}{1000} \right) + 1 \right] = 1.26 \text{ Volt}$$

MCP61P 1.2V + 1.2V_HT = 7.6725A

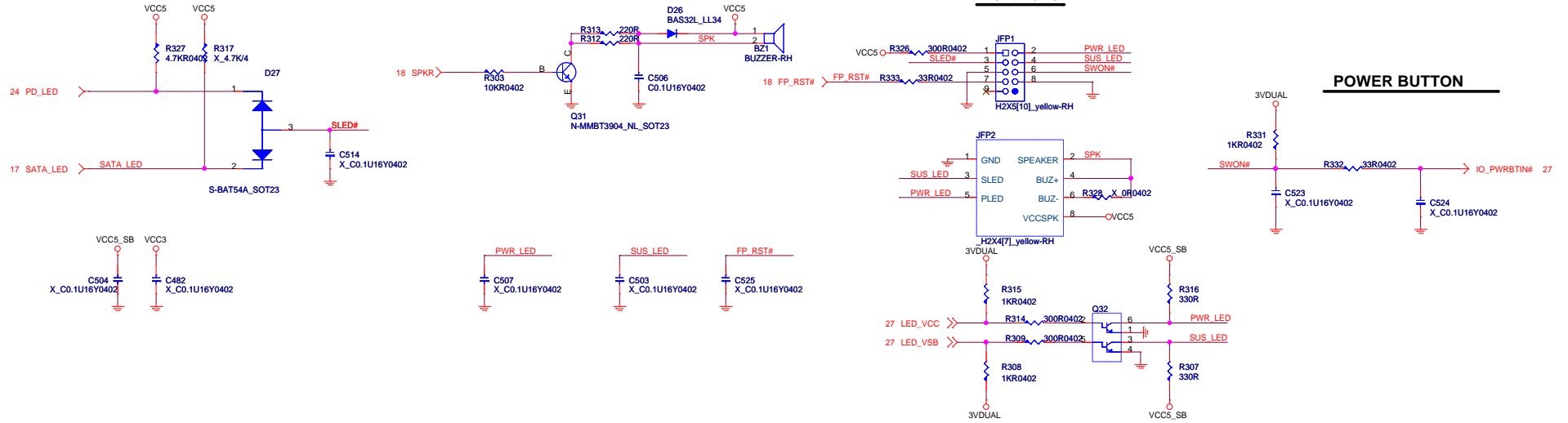
1124_11 (1124_1 : 0.50mm / 1) GAB = 100 mm

$$V_{out} : 1.25 [(200 / 1000) + 1] = 1.5 \text{ Volt}$$
$$V_{out} : 1.2 \left[\left(75 / 300 \right) + 1 \right] = 1.5 \text{ Volt}$$
$$V_{out} : 1.5 \left[\left(75 / 300 \right) + 1 \right] = 1.875 \text{ Volt}$$

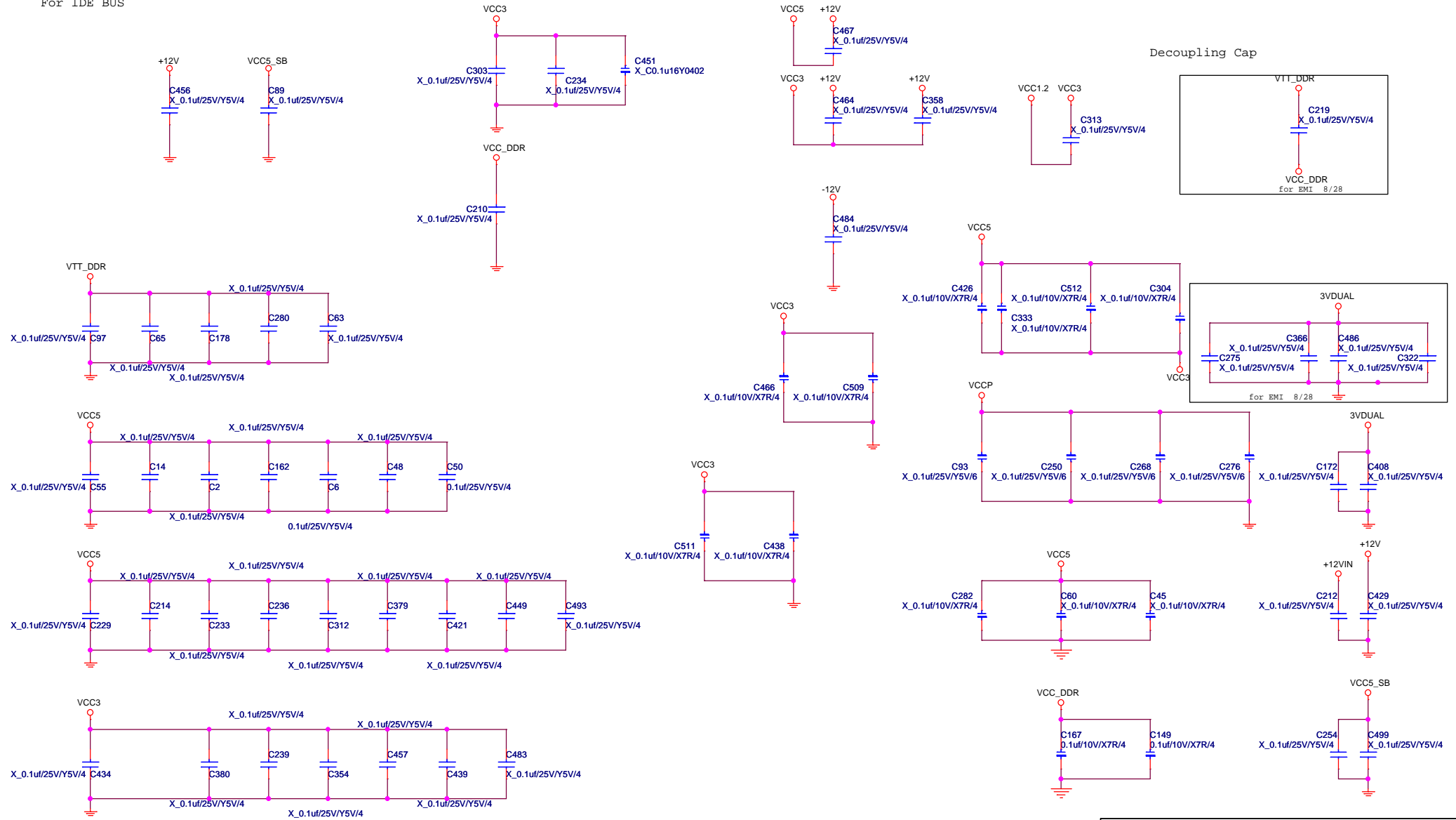
ATX Connector



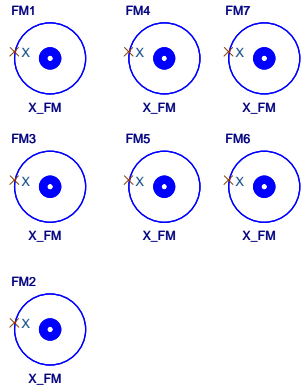
Front Panel



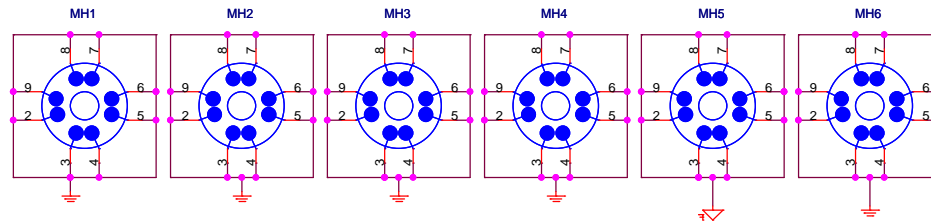
For IDE BUS



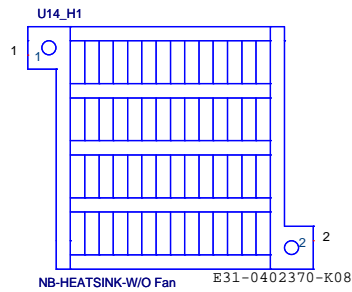
Optics Orientation Holes



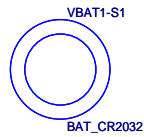
Mounting Holes



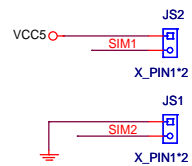
NB FAN/HEAT-SINK



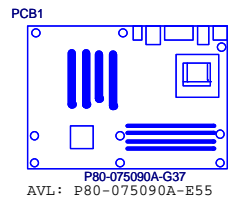
BATTERY




Simulation



PCB



		MICRO-START INTL CO.,LTD.	
Title		BOM - Option Parts	
Size	Document Number	Rev	
Custom	MS-7509	0A	
Date:	Tuesday, October 02, 2007	Sheet	34 of 37

ATX P/S WITH 1A STBY CURRENT						CPU PW
VBAT	5VSB +/-5%	5V +/-5%	3.3V +/-5%	12V +/-5%	-12V +/-5%	12V +/-5%

VRM SW
REGULATOR

CPU_VCORE (S0, S1)

VDD 1.5V
REGULATOR

VDD 1.3 V
REGULATOR

AM2 ATHLON 64	
VCORE	0.8-1.55V 80A(90W)
VTT_DDR	1.75A
VCC_DDR	3.6.A
VCC1_2HT	1.25V 0.5A

VTT_DDR(S0,S1,S3)
VCC_DDR(S0,S1,S3)
VCC1_2HT (S0, S1)

VCC1_2HT(S0,S1)

MCP61

VCC1_2HT	1.3V 7.5A
VCC3	0.615A
3VDUAL	0.556A
1.2VDUAL	0.225A
VBAT(G3,S0,S1,S3,S4,S5)	VBAT 5mA(S0,S1)/ 100uA(S3,S5)/ 10uA(G3)

+3.3V (S0, S1)

3VDUAL (S0, S1, S3, S4, S5)

1.2VDUAL (S0, S1, S3, S4, S5)

VBAT(G3,S0,S1,S3,S4,S5)

VTT_DDR(S0,S1,S3)

VCC_DDR(S0,S1,S3)

DDR400 DIMMs	
VTT_DDR	0.3A/DIMM (0.6A)
VCC_DDR	2.6A/DIMM (5.2A)

0.9V VTT_DDR
REGULATOR

1.8V VCC_DDR
REGULATOR

+3.3VDUAL REGULATOR
ACPI CONTROLLER

3VDUAL (S0, S1, S3, S4, S5)

+5VSB REGULATOR
ACPI CONTROLLER

+5V_Dual (S0, S1, S3)

1.2V STB
REGULATOR

1.2VDUAL (S0, S1, S3, S4, S5)

VBAT(G3,S0,S1,S3,S4,S5)

VCC3 (S0, S1)

VT6308P 1394	
VCC3	

AC97 CODEC	
VCC3 (S0, S1)	3.3V
+5VR (S0, S1)	5V

3VDUAL (S0, S1, S3, S4, S5)

LAN	
3VDUAL	
AVDD18	
AVDD15	

3VDUAL (S0, S1, S3, S4, S5)

SUPER I/O	
3VDUAL	
VCC3 (S0, S1)	
VBAT	

VCC3 (S0, S1)

VBAT

+5V_Dual (S0, S1, S3)

PCI Slot (per slot)	
5V	5.0A
3.3V	7.6A
12V	0.5A
3.3Vaux	0.375A
-12V	0.1A

X2

+3.3VDUAL (S0, S1, S3)

X1 PCIE		X16 PCIE	
3.3V	3.0A	3.3V	3.0A
12V	5.5A	12V	5.5A

1394 FR*1		1394 RL*1	
12V	1.5A	12V	1.5A

USB FR*4	
5VDual	2A

USB RL*4	
5VDual	2A

PS/2	
5VDual	1A

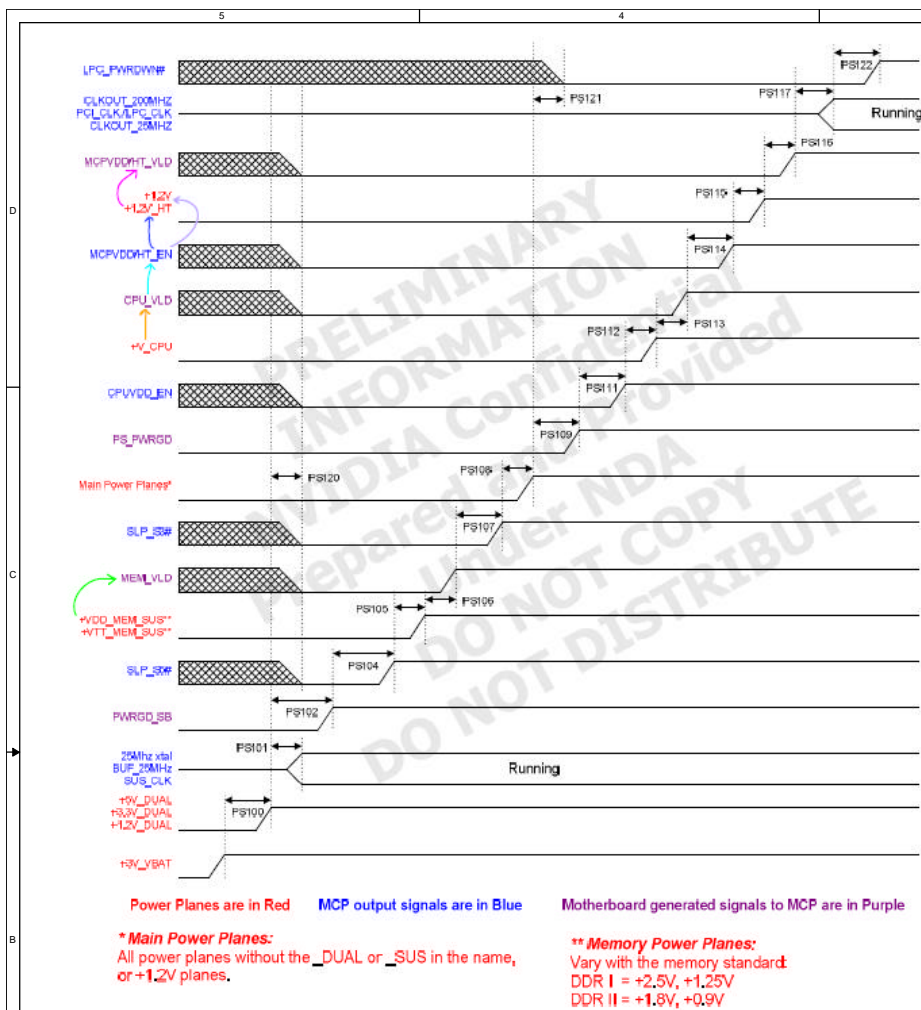


Figure 4-2. MCP68 G3-to-S0 Power-Up Sequence

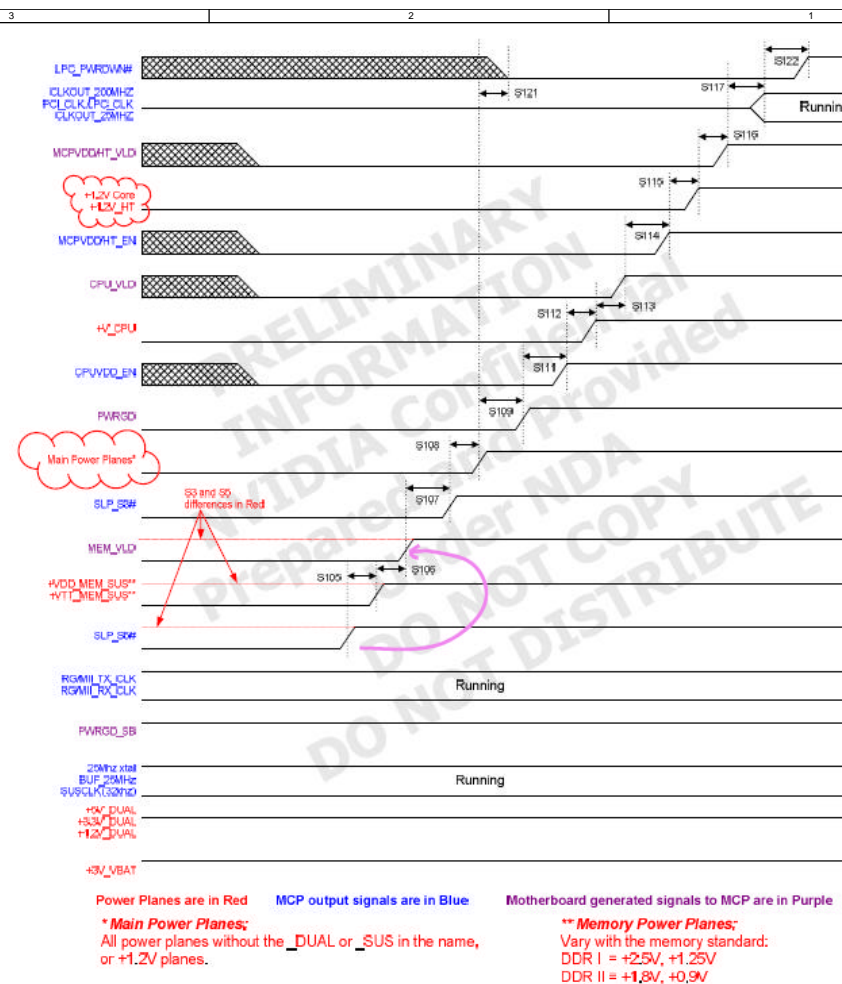


Figure 4-3. MCP68 S3/S4/S5 Power Resume Sequence

2006/11/14 0A



MICRO-START INT'L CO.,LTD.

Title			HISTORY		
Size	Document Number		Rev		
Custom	MS-7509		0A		
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